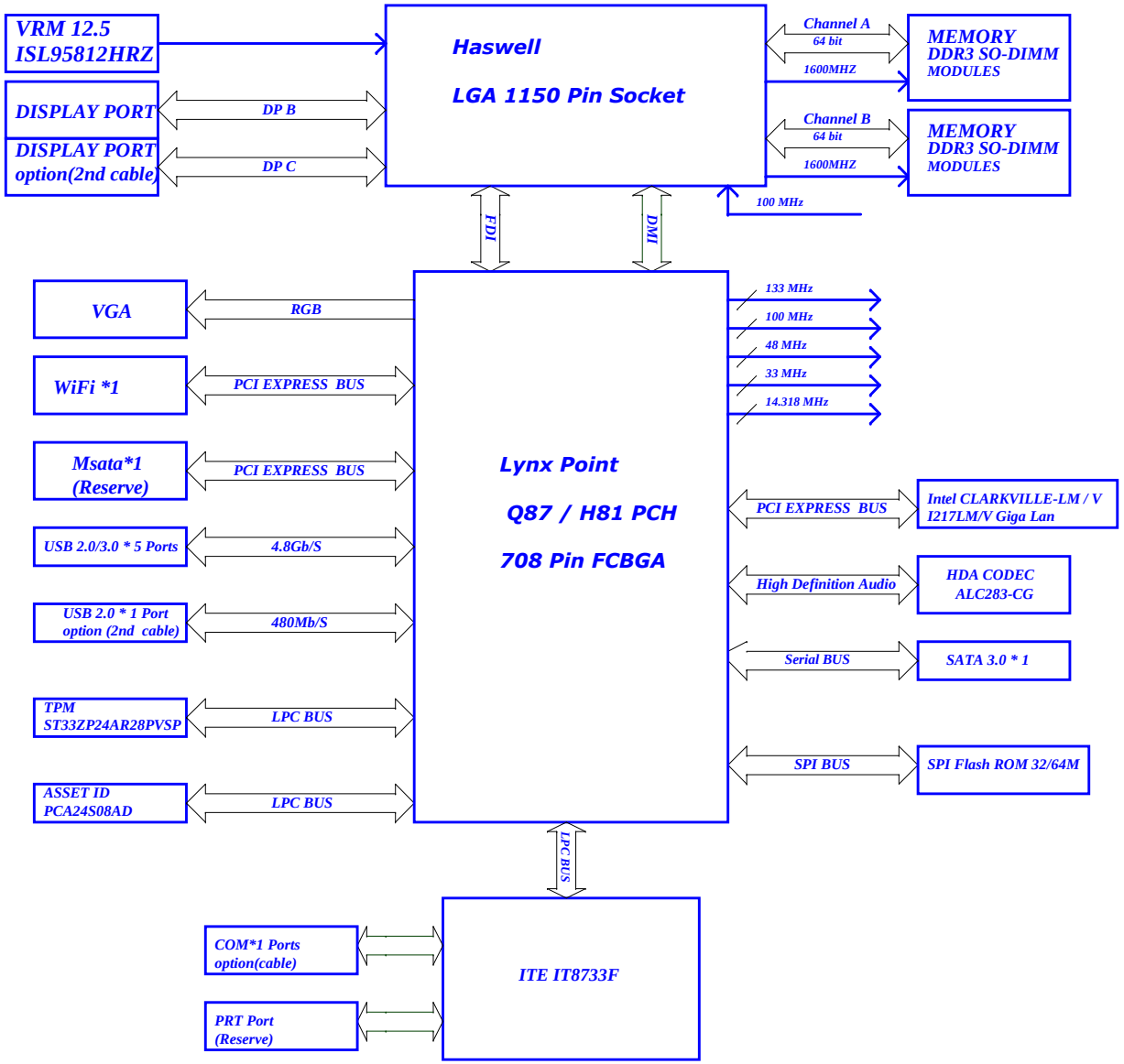
JC184 / JC186

Project JC184/JC186

Document No : A116/A1232

A01 : 2013/03/07



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11	Blank
12	DDR3 CHB SO-DIMM3
13	Blank
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28	Display Port B
29	Display Port C
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32	TPM - ST ST33ZP24AR28PVSH
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34	USB3.0 ODD CONN / Int USB
35	USB3.0 CONN x 3
36	USB3.0 x1/ USB CHARGER
37	Mini PCIE/ 2 COM PORT
38	MSATA
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43	PWRGD & Bleed Off
44	Button/LED
45	SM BUS/Thermal Sensing/APS
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47	Mounting Hole
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49	DC +19V_MAIN / POWER METER
50	+5V_DUAL / +3_3V_DUAL
51	+5V/ +3.3V/ +3_3V_LPS/ ME
52	+12V
53	VCORE CONTROLLER
54	VCORE OUTPUT
55	+1.5V_DDR / +VTT_DDR
56	+1.5_PCH / +1_05PCH
57	+1_05V_ME / +5V_USB
58	STRAPPING PIN
59	PCH GPIO TABLE
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61	Change List
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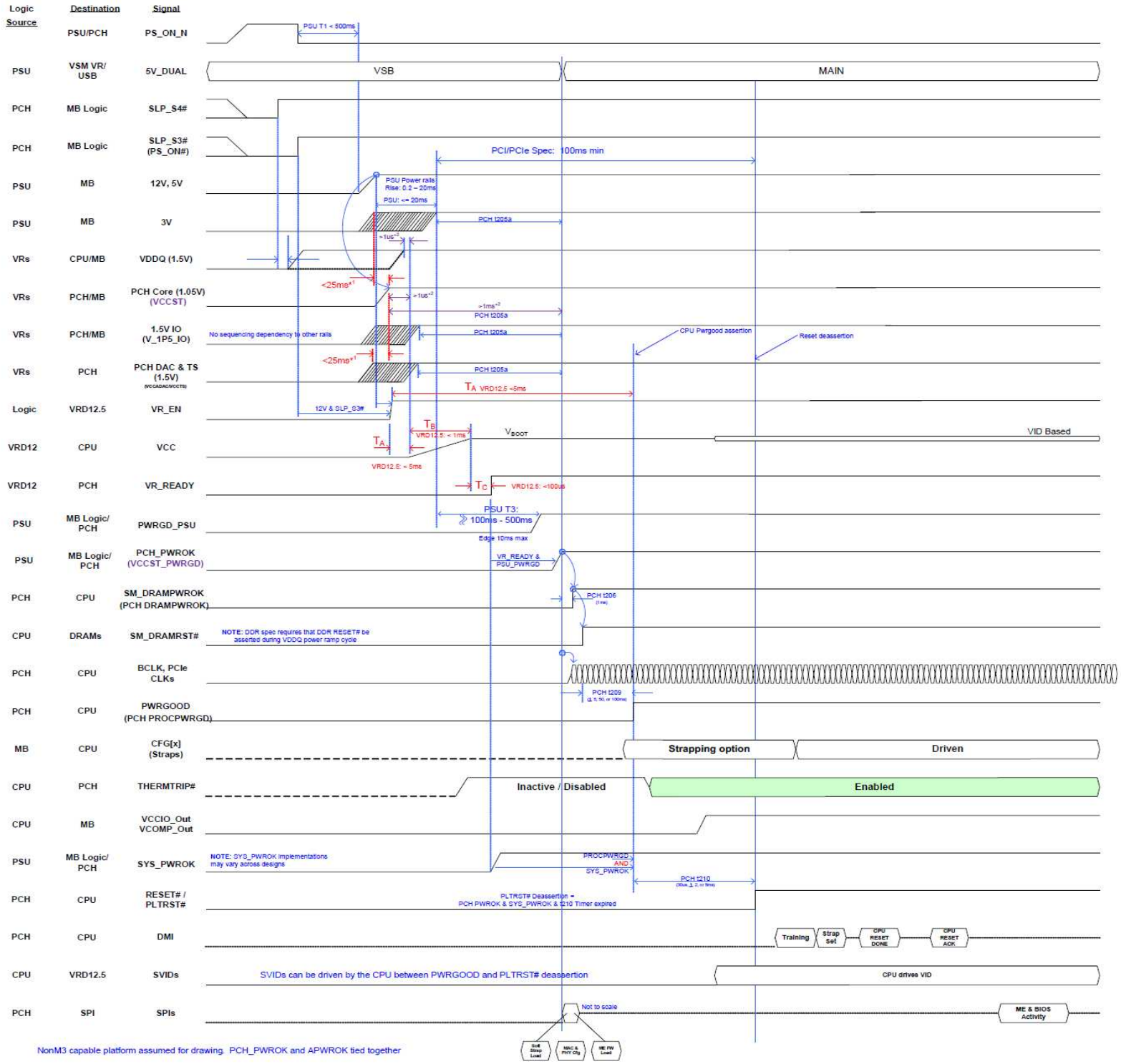

LITE-ON TECHNOLOGY CORP.			LITEON
Title	02. Power Sequence		
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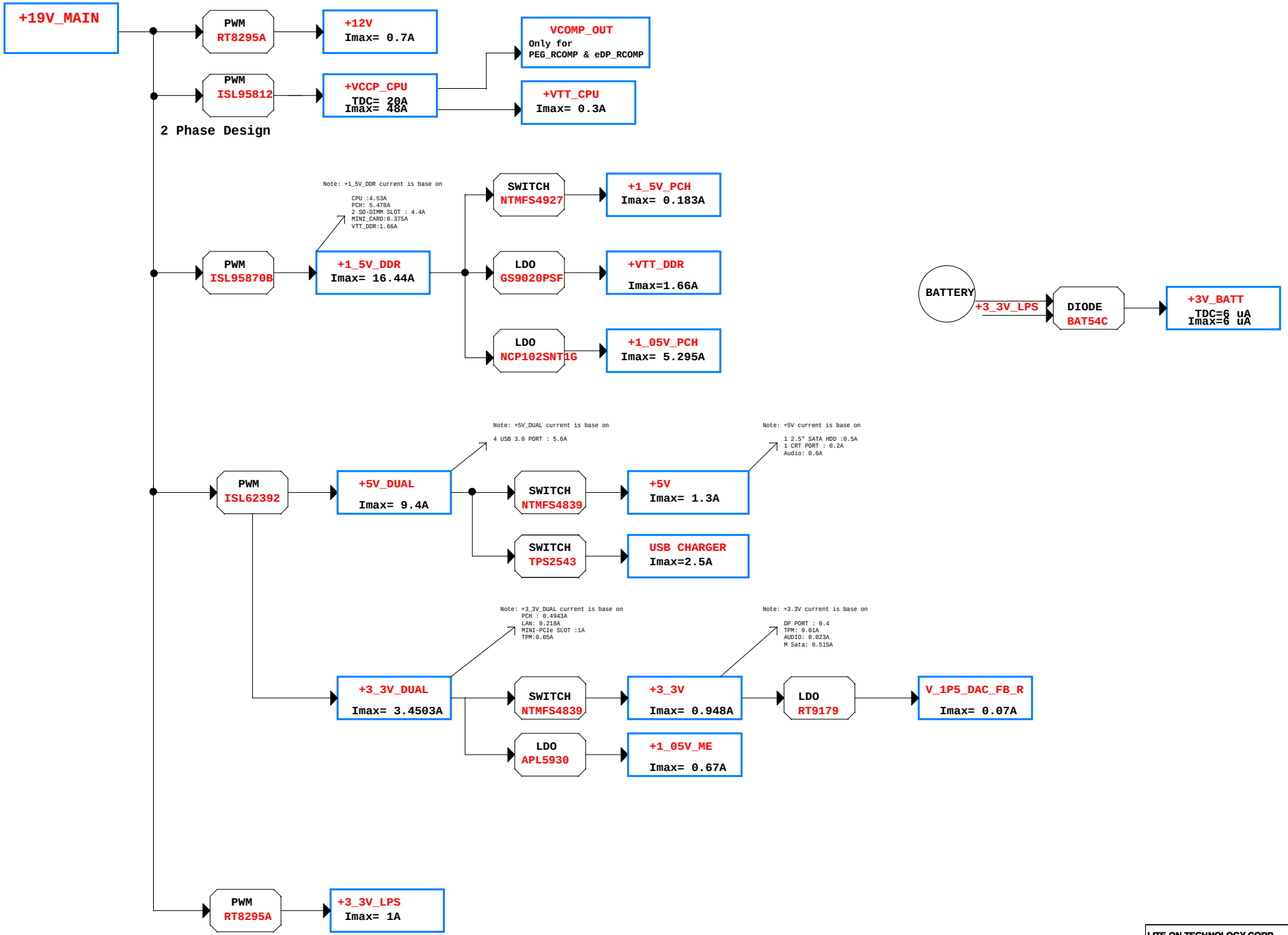
POWER CONN



LITE-ON TECHNOLOGY CORP.		LITEON
Title	03. Power Delivery Map	
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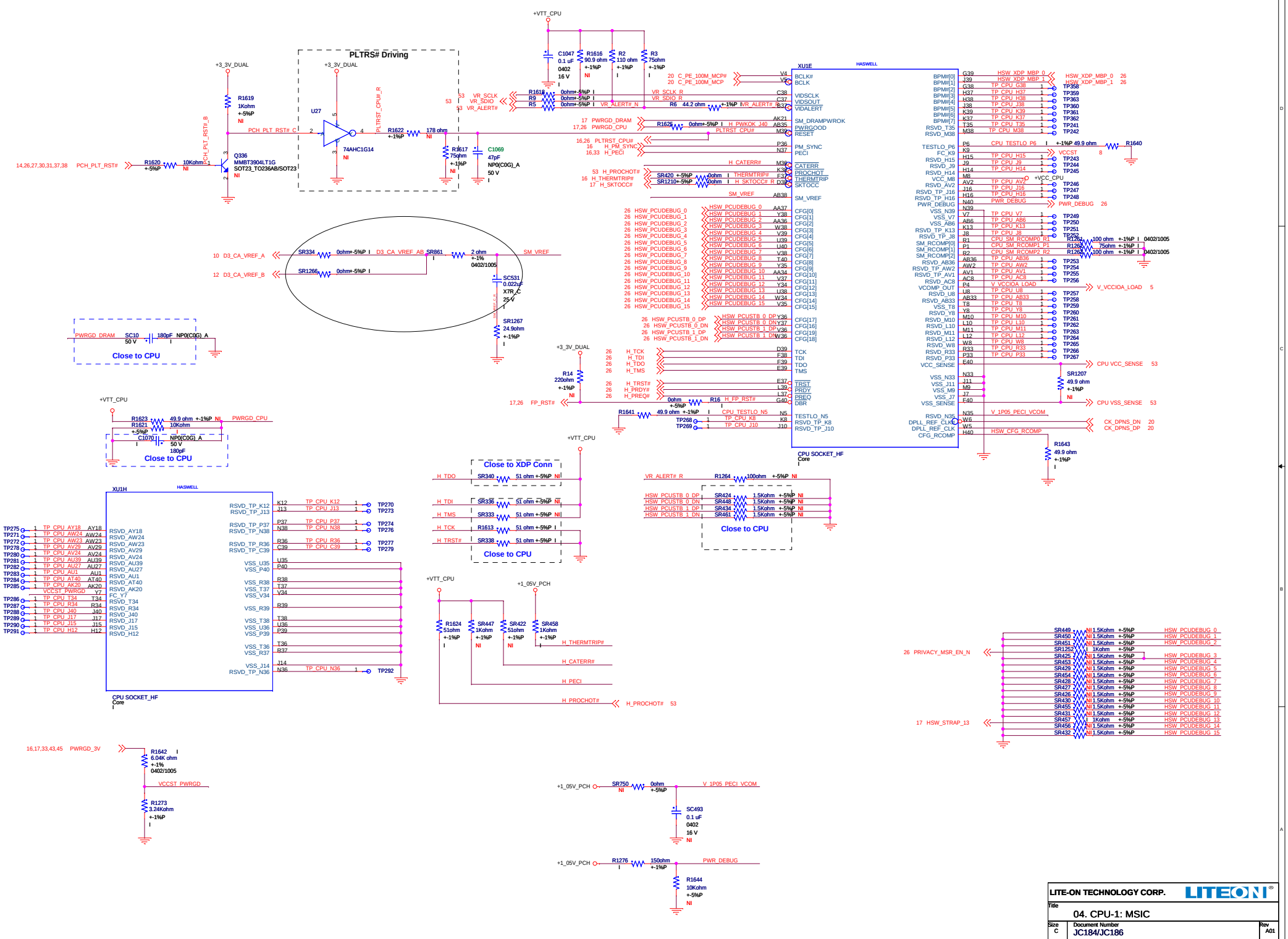
PLTRS# Driving
XU1E
HASWELL
CPU SOCKET_HF
Core
XU1H
Close to CPU
Close to XDP Conn
LITE-ON TECHNOLOGY CORP.
Title
04. CPU-1: MSIC
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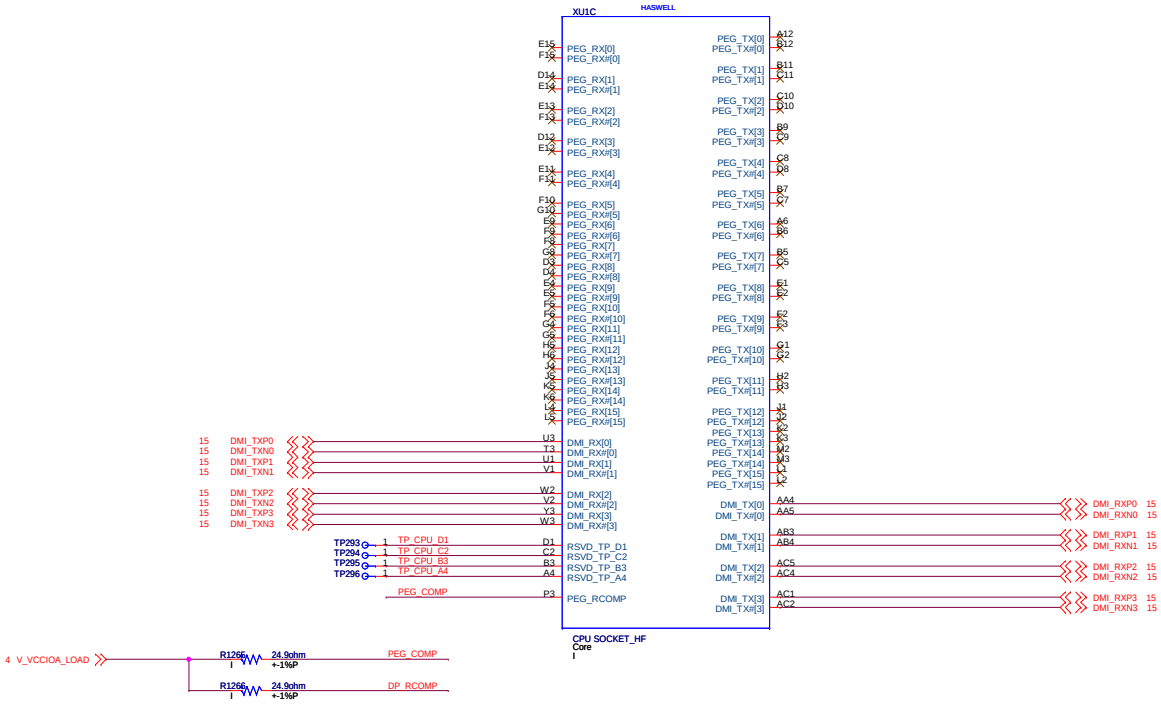

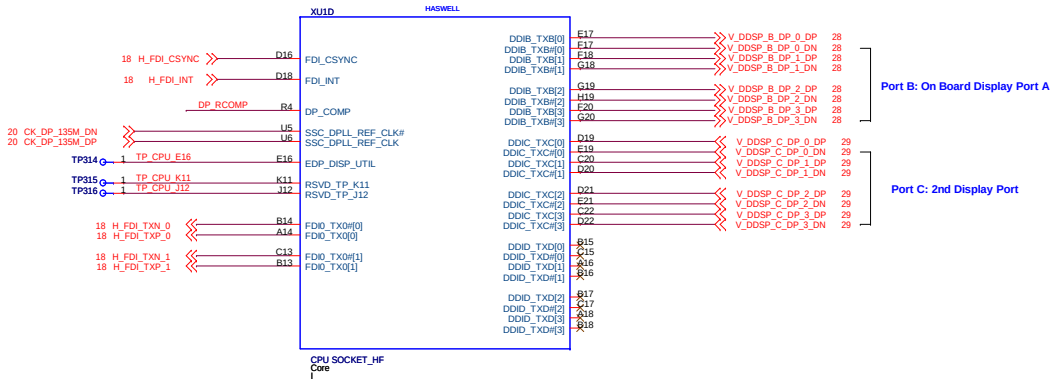

LITE-ON TECHNOLOGY CORP.			LITEON
Title	05. CPU-2: FDI/PCIe/DMI		
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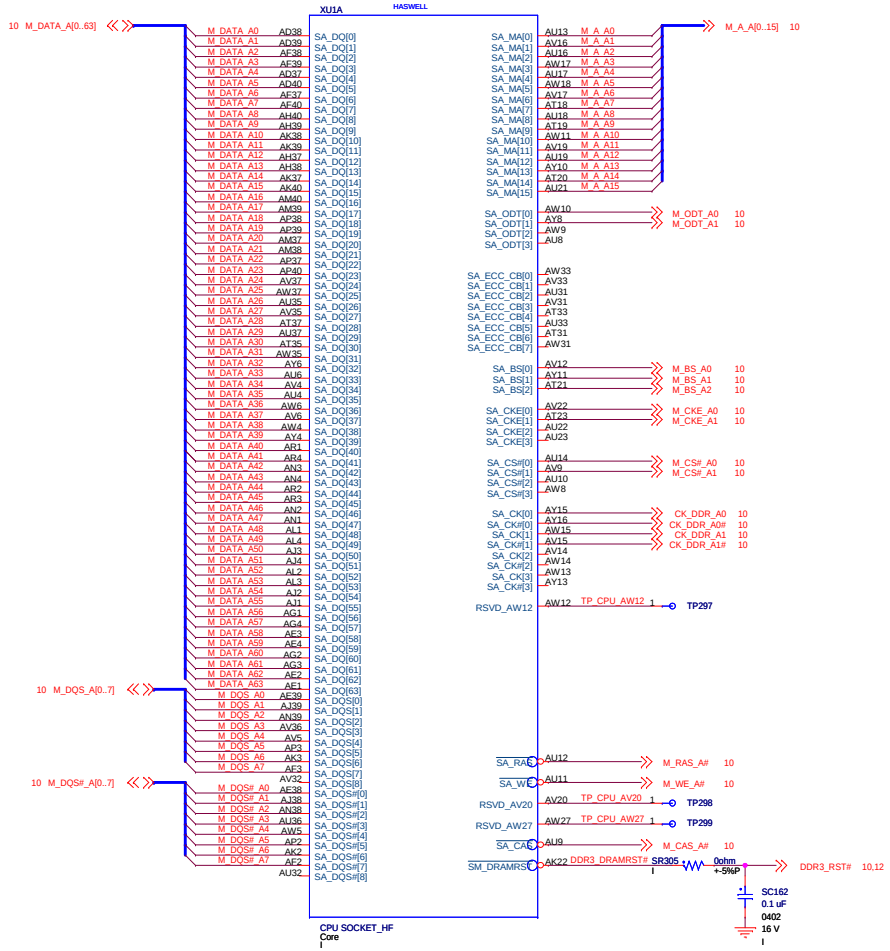

LITE-ON TECHNOLOGY CORP.

Title: 06. CPU-3: DDR3_CHA

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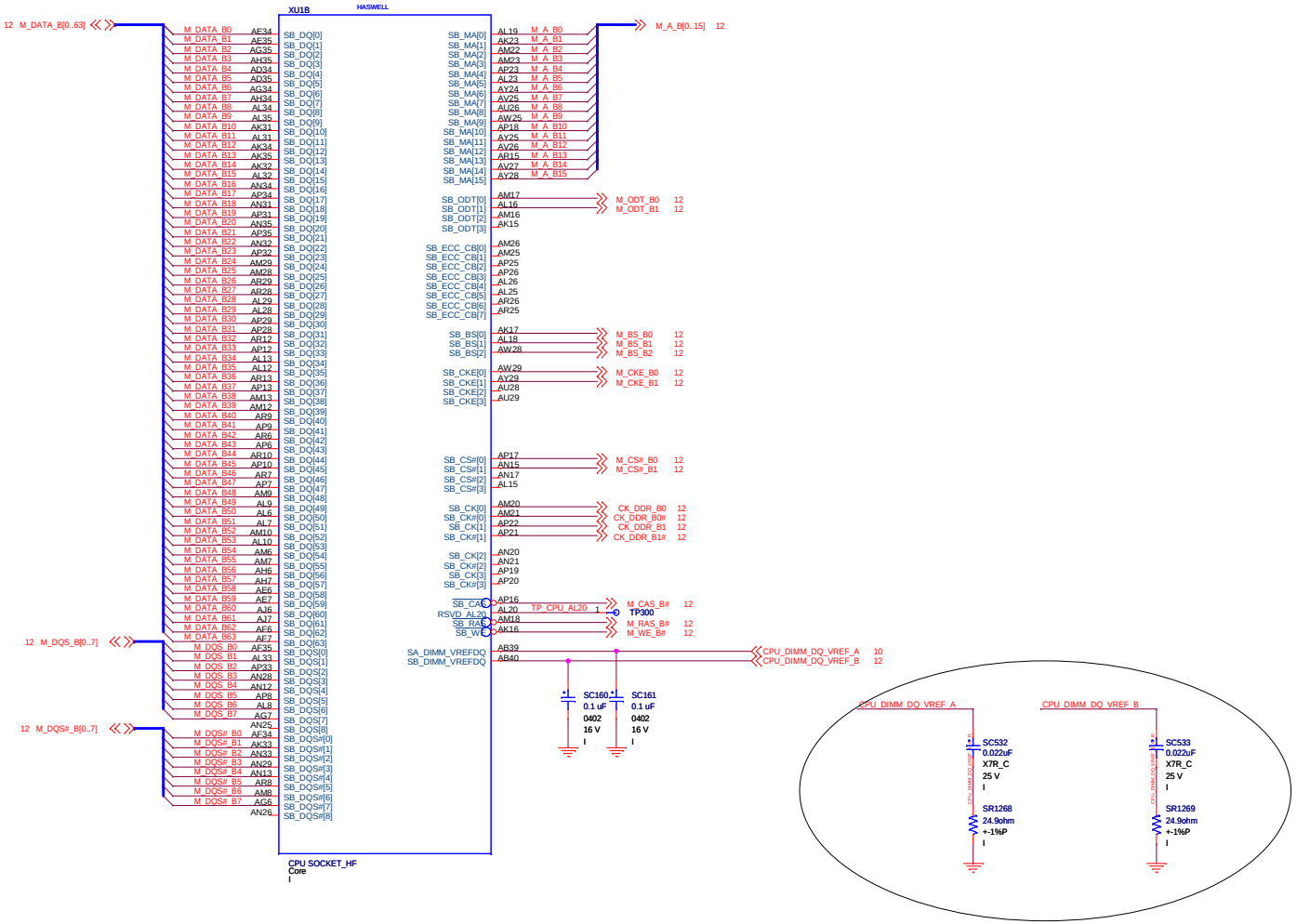

LITE-ON TECHNOLOGY CORP.		LITEON
Title	07. CPU-4: DDR3_CHB	
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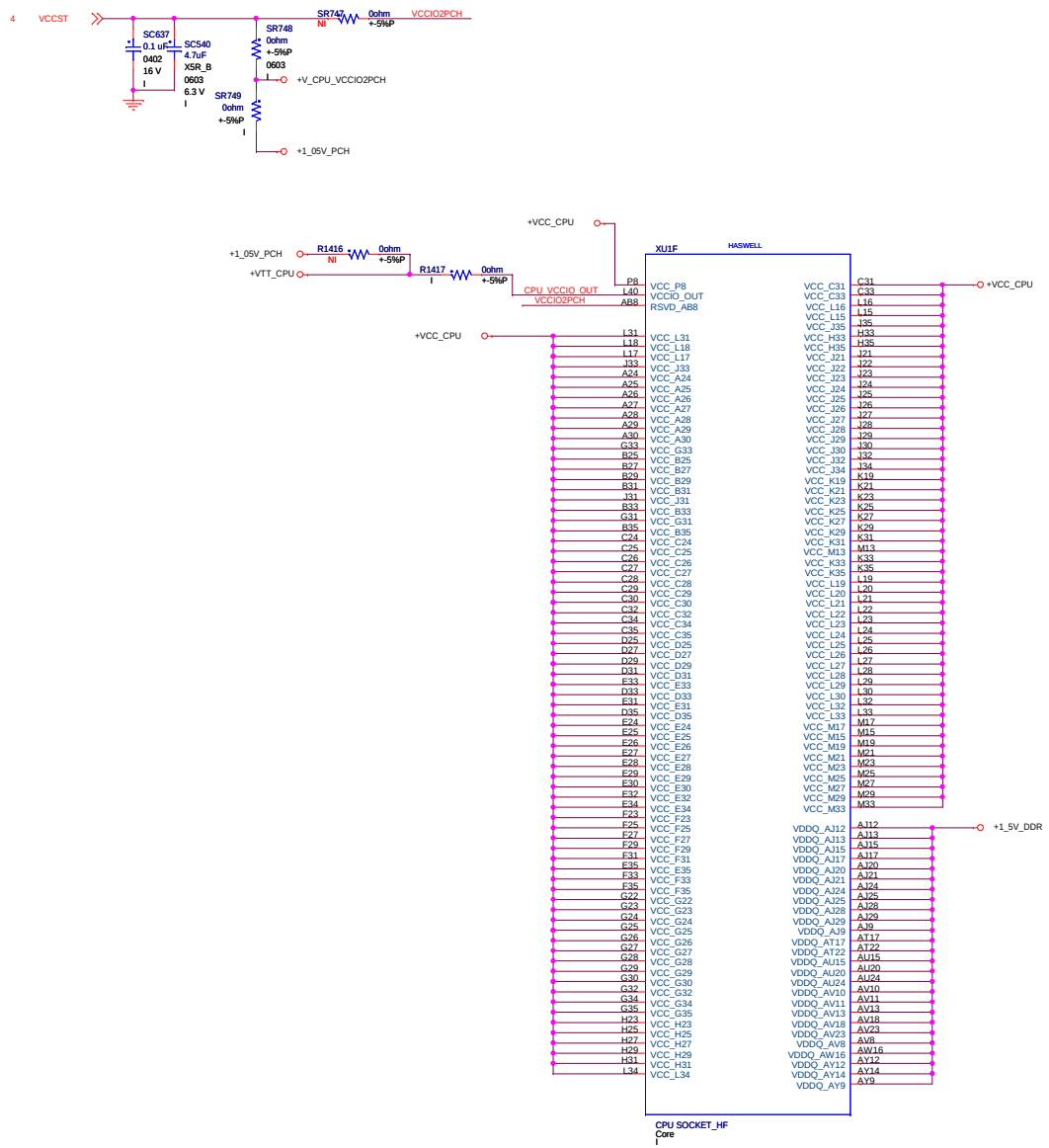

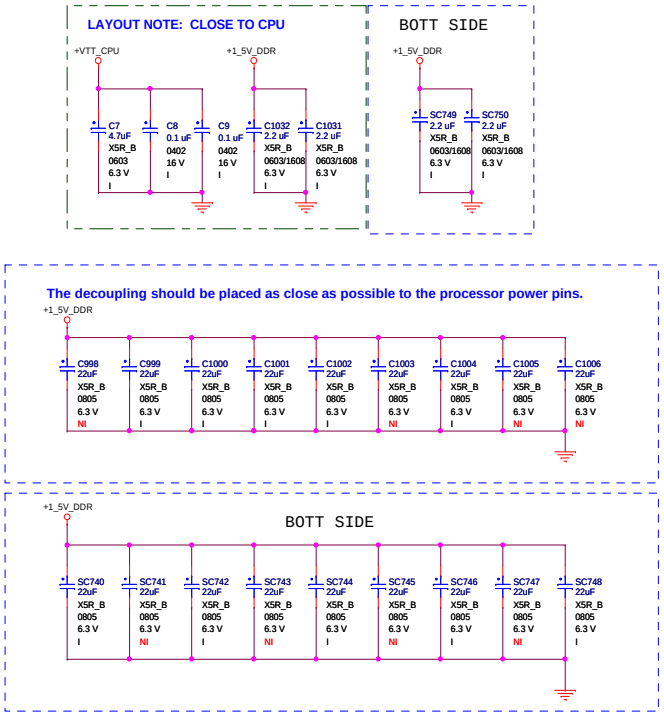

LITE-ON TECHNOLOGY CORP.		LITEON
Title	08. CPU-5: Power	
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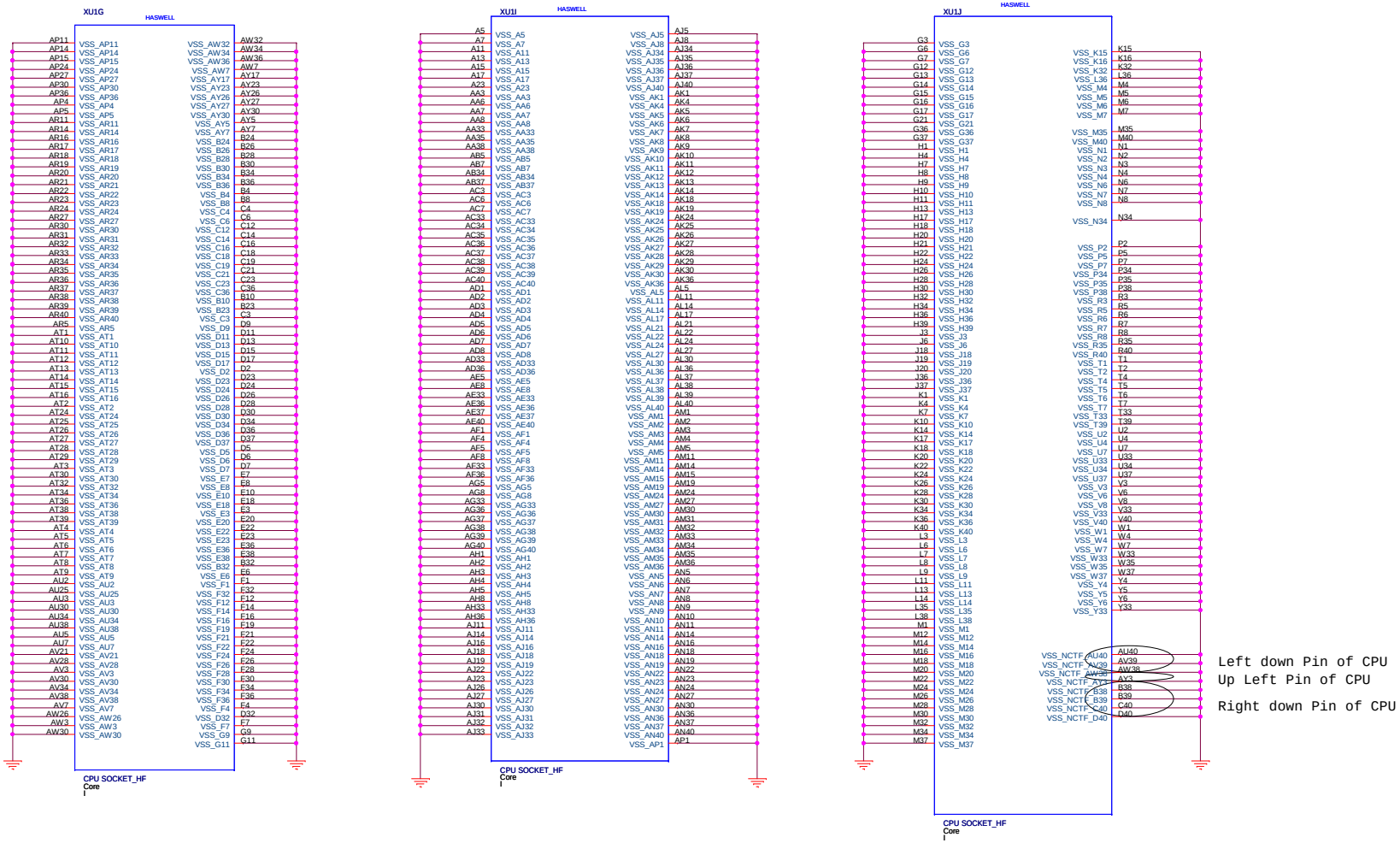

LITE-ON TECHNOLOGY CORP.

Title: 09. CPU-6: GND

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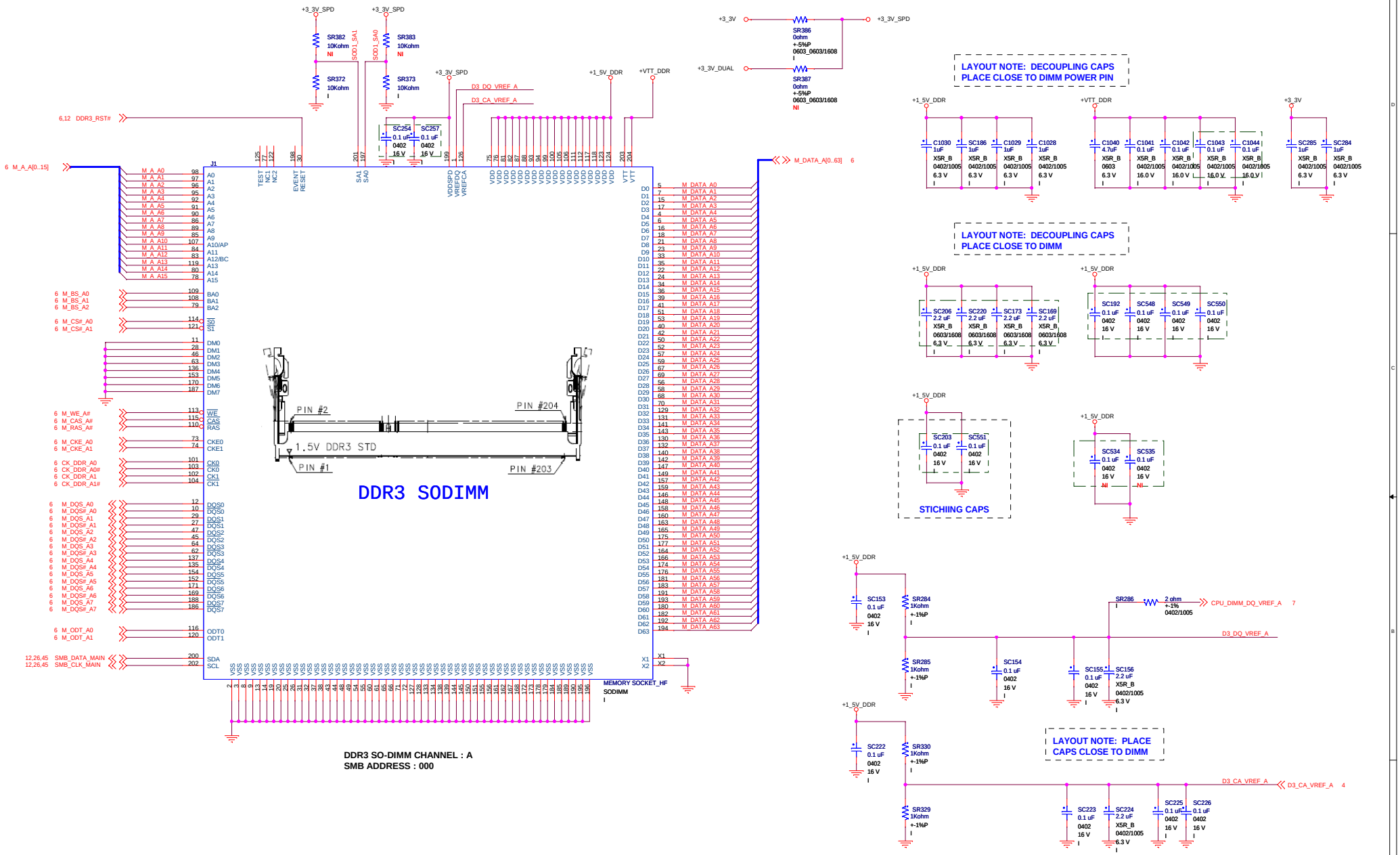

LITE-ON TECHNOLOGY CORP.

Title: 10. DDR3 CHA SO-DIMM1

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LITE-ON TECHNOLOGY CORP.

Title

11. Blank

Size	Document Number	Rev
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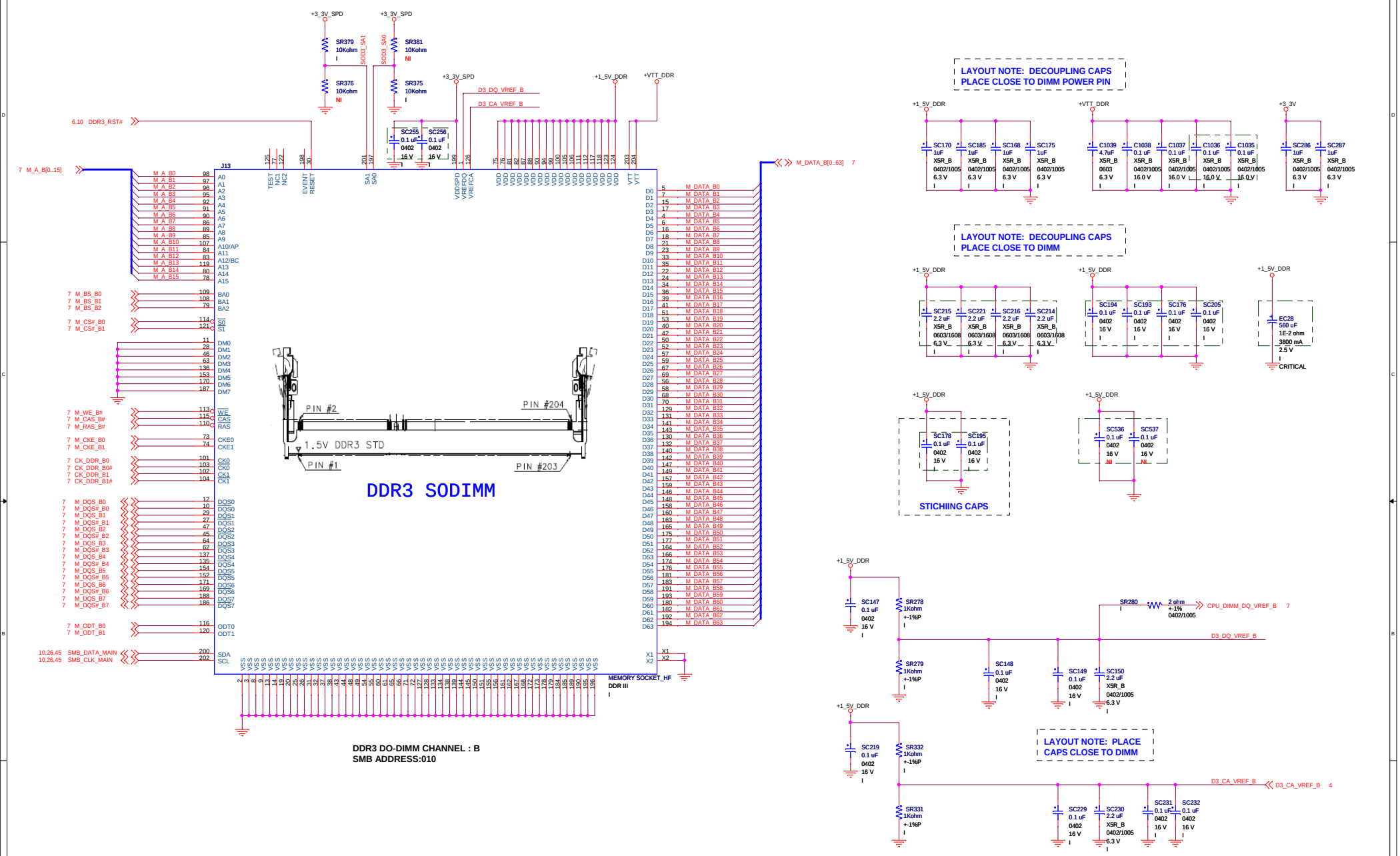

LITE-ON TECHNOLOGY CORP.

Title: 12. DDR3 CHB SO-DIMM3

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Title

13. Blank

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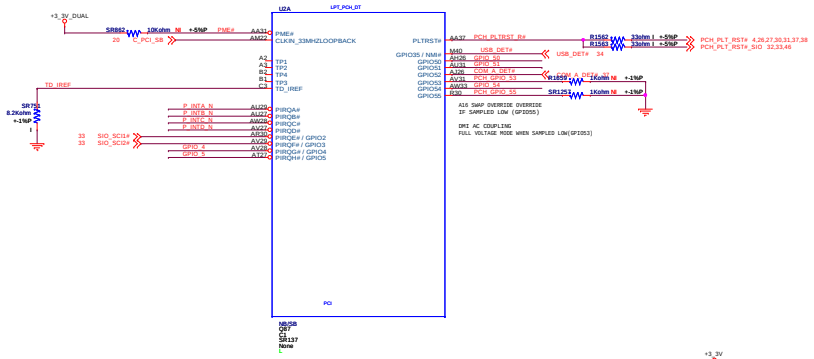
Option for H81
L:Q87 Install
M:Q87 NI for H81

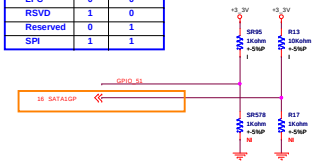
U2_
H81
PCH H81
NA
M

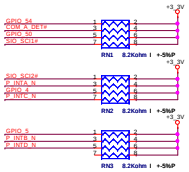
No PCI Device



Boot BIOS Select

Boot Device	GPIO51	SATA1GP
LPC	0	0
RSVD	1	0
Reserved	0	1
SPI	1	1





LITE-ON TECHNOLOGY CORP.			LITEON
Title	14. PCH-1: PCI		
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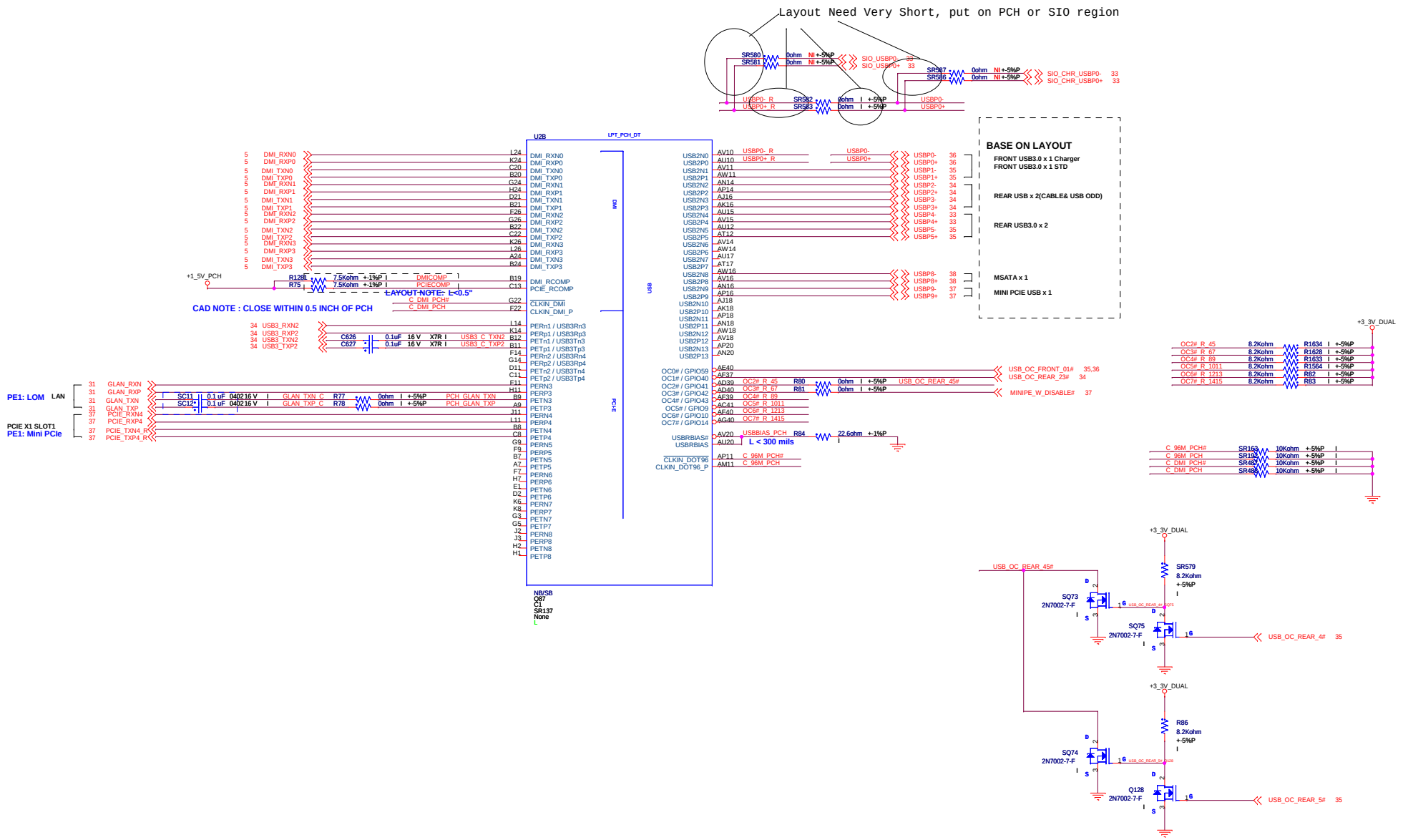

LITE-ON TECHNOLOGY CORP.

Title: 15. PCH-2: DMI/PCIe/USB

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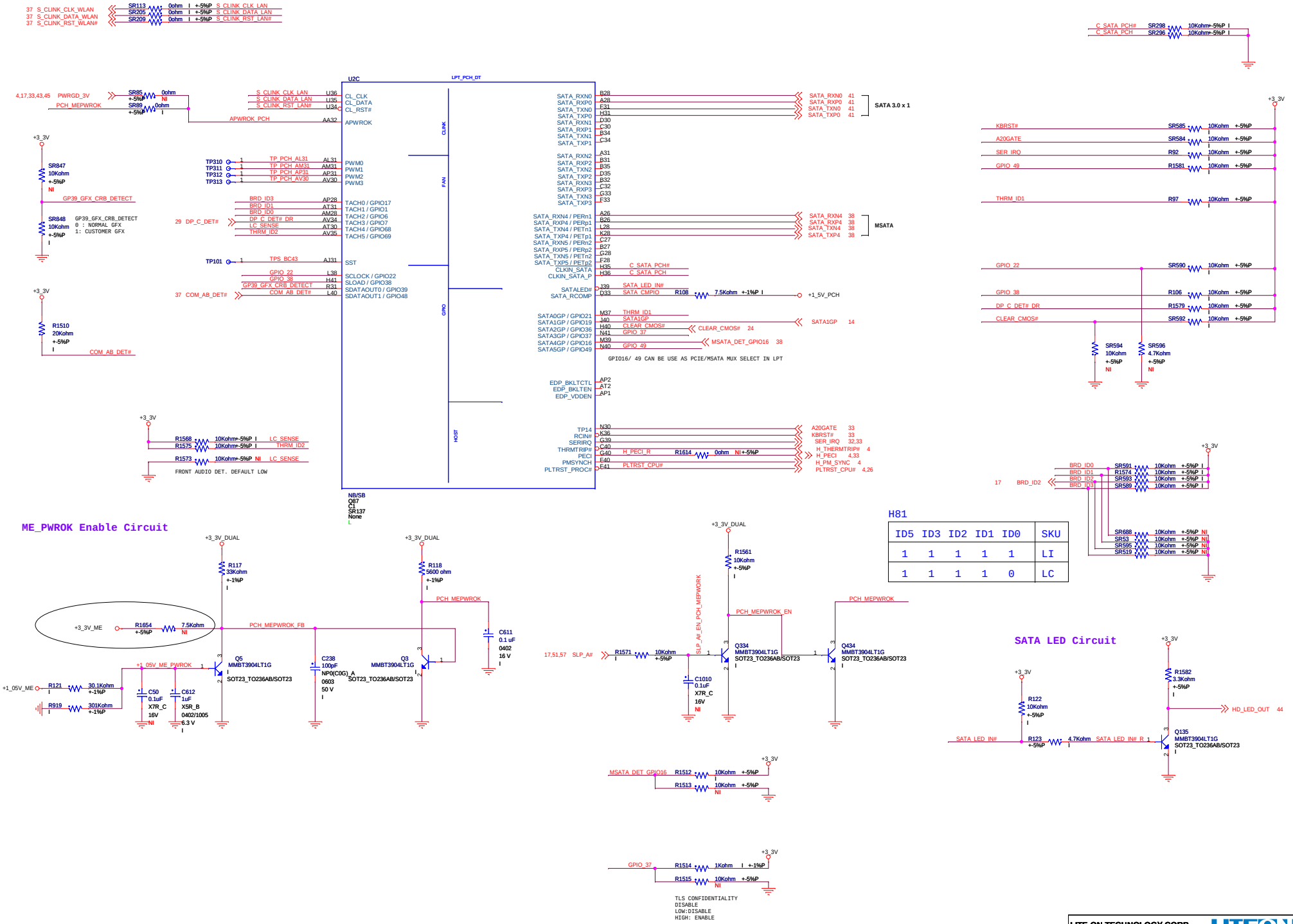

LITE-ON TECHNOLOGY CORP.

Title: 16. PCH-3: SATA/HOST/FAN

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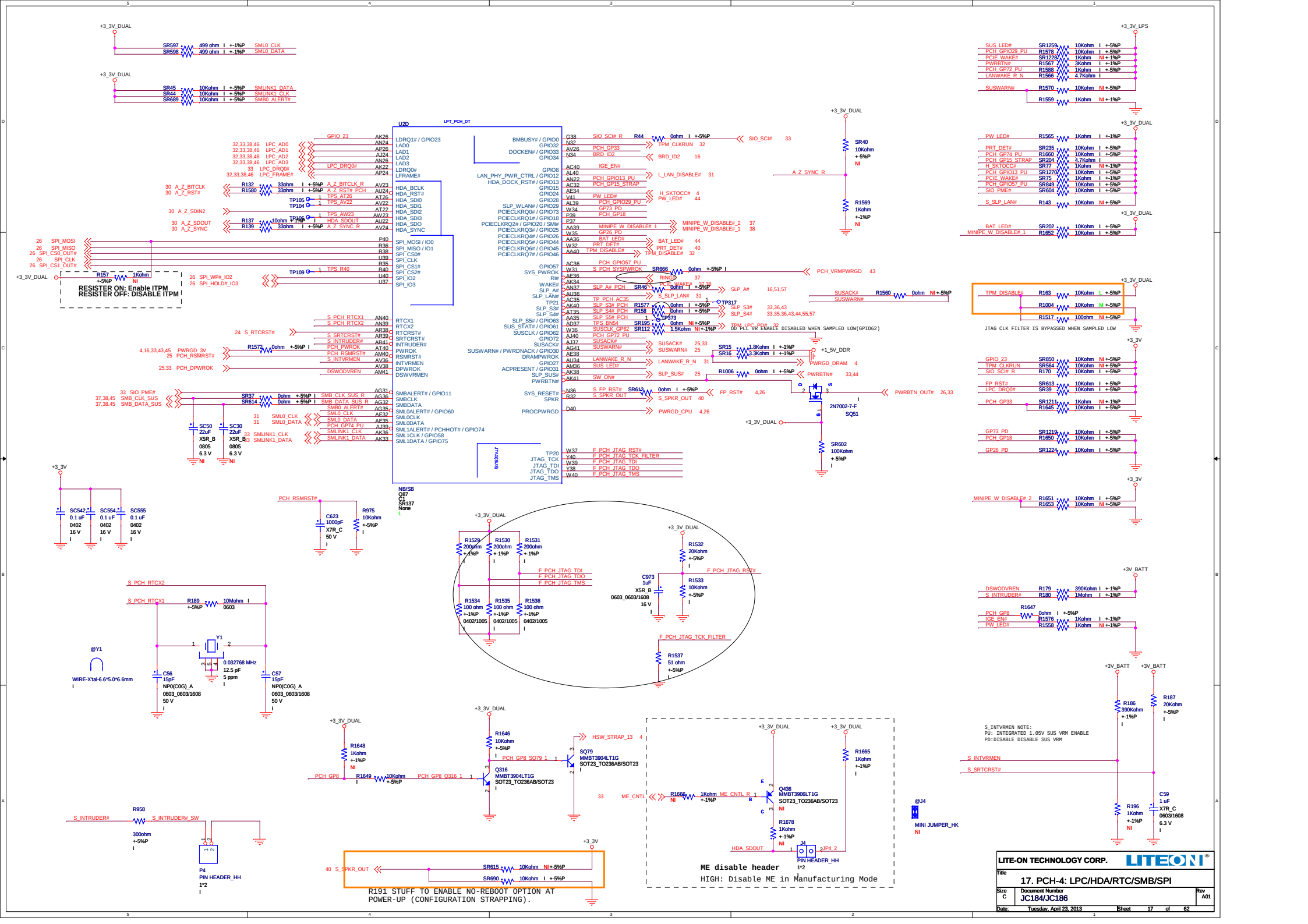
U2D
LPT_PCH_DT
NB/SB
Q87
C1
SR137
None
RESISTER ON: Enable ITPM
RESISTER OFF: DISABLE ITPM
JTAG CLK FILTER IS BYPASSED WHEN SAMPLED LOW
OD PLL VR ENABLE DISABLED WHEN SAMPLED LOW(GPIO62)
S_INTVRMEN NOTE:
PU: INTEGRATED 1.05V SUS VRM ENABLE
PD:DISABLE DISABLE SUS VRM
ME disable header
HIGH: Disable ME in Manufacturing Mode
R191 STUFF TO ENABLE NO-REBOOT OPTION AT
POWER-UP (CONFIGURATION STRAPPING).
LITE-ON TECHNOLOGY CORP.
Title
17. PCH-4: LPC/HDA/RTC/SMB/SPI
Size C
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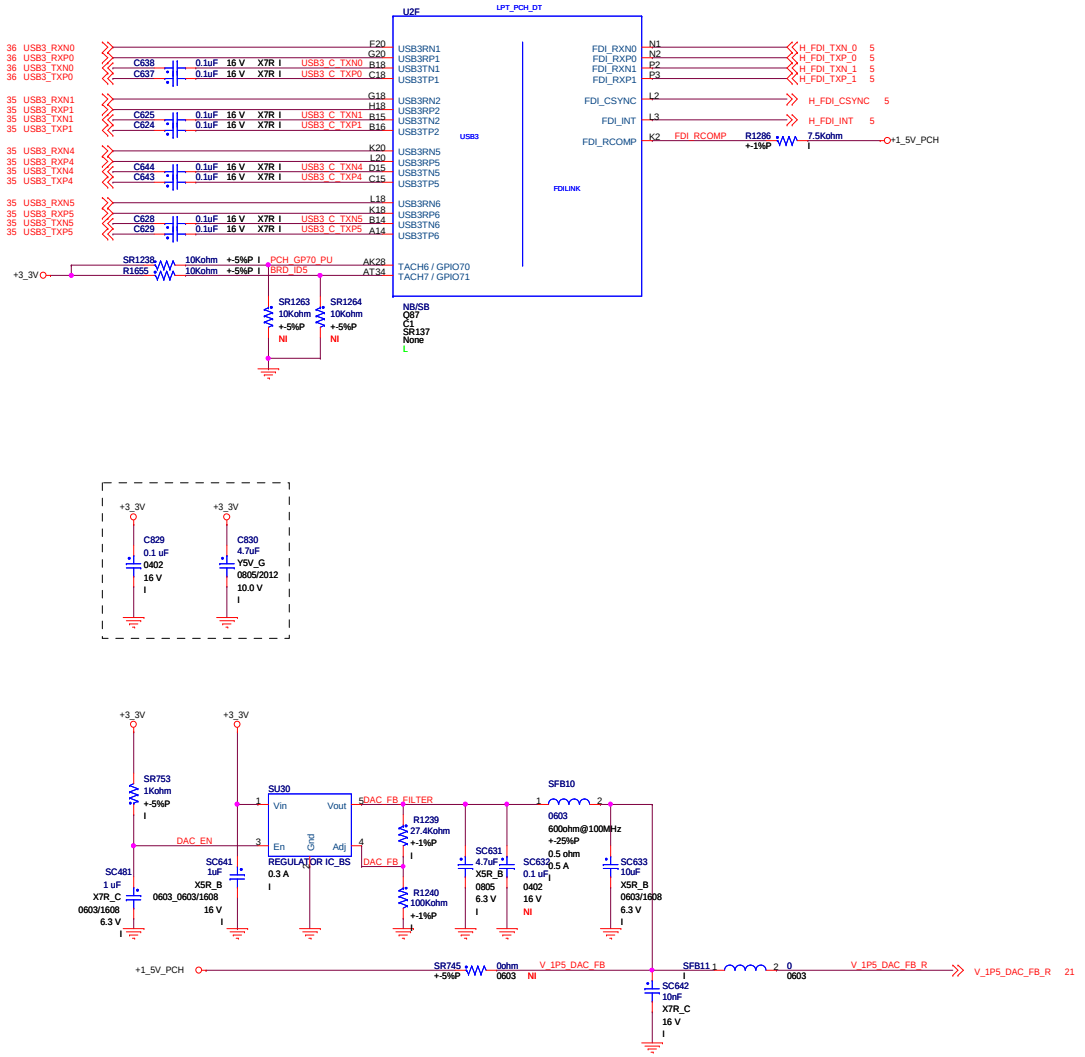

LITE-ON TECHNOLOGY CORP.		LITEON
Title	18. PCH-5/7: NVRAM/FDI	
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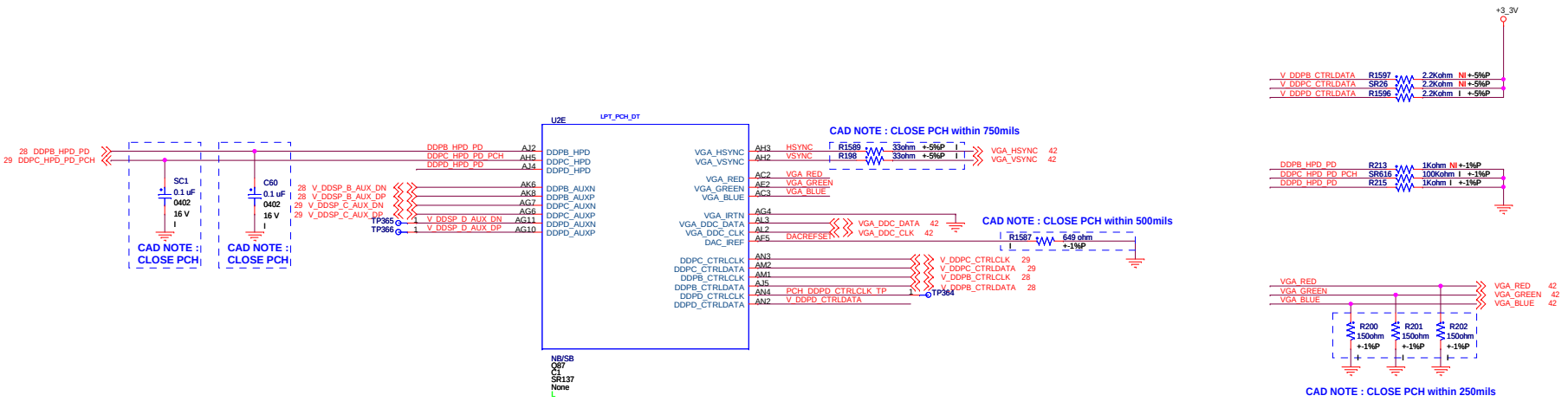

LITE-ON TECHNOLOGY CORP.			
Title	19. PCH-6: Display		
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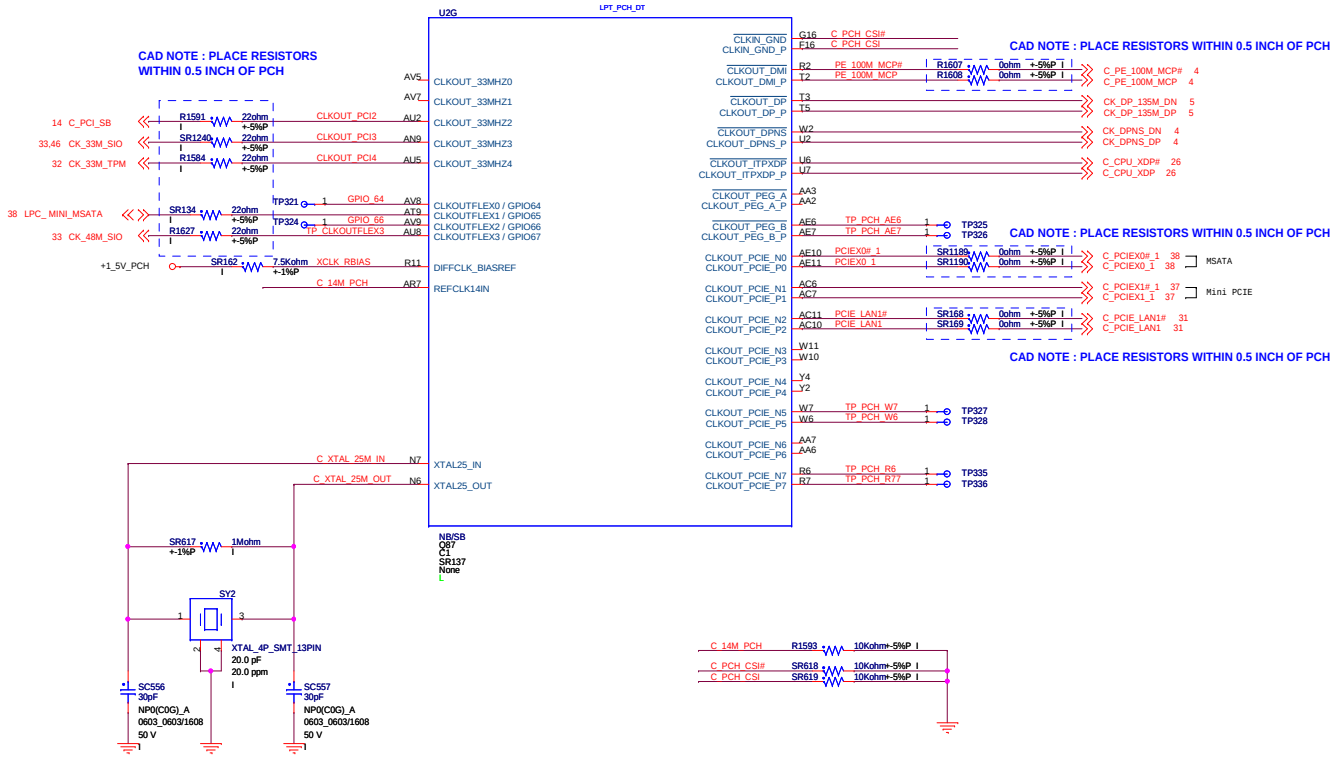

LITE-ON TECHNOLOGY CORP.		LITEON
Title	20. PCH-8: Clock	
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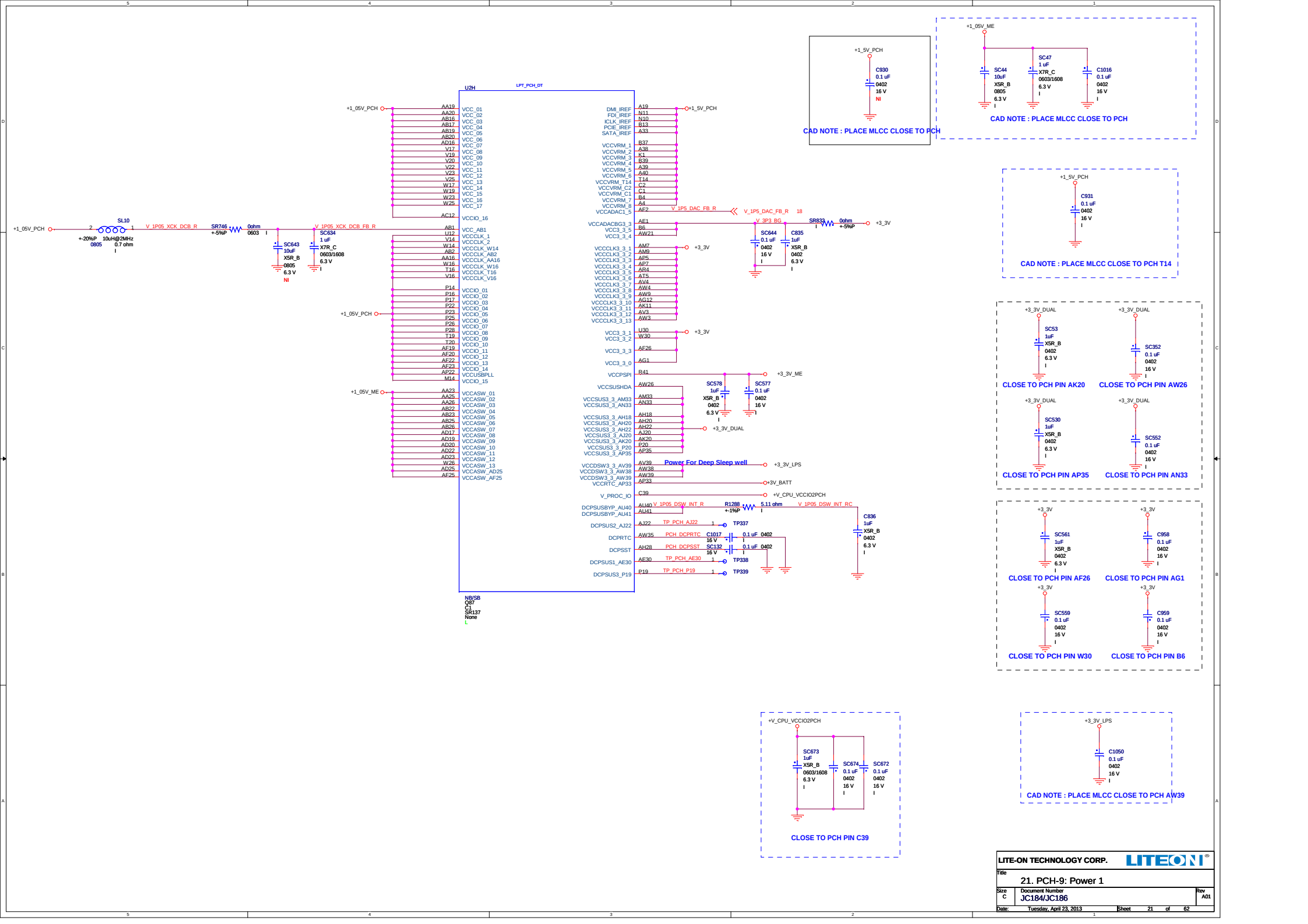
U2H
LPT_PCH_DT
+1_05V_PCH
SL10
+-20%P 10uH@2MHz
0805 0.7 ohm
V_1P05_XCK_DCB_R
SR746 0ohm
+-5%P 0603
V_1P05_XCK_DCB_FB_R
SC643 10uF X5R_B 0805 6.3 V NI
SC634 1 uF X7R_C 0603/1608 6.3 V
+1_05V_ME
+1_5V_PCH
V_1P5_DAC_FB_R
V_1P5_DAC_FB_R 18
V_3P3_BG
SR833 0ohm
+-5%P
+3_3V
SC644 0.1 uF 0402 16 V
C835 1uF X5R_B 0402 6.3 V
+3_3V_ME
SC578 1uF X5R_B 0402 6.3 V
SC577 0.1 uF 0402 16 V
+3_3V_DUAL
Power For Deep Sleep well
+3_3V_LPS
+3V_BATT
+V_CPU_VCCIO2PCH
V_1P05_DSW_INT_R
R1288 5.11 ohm
+-1%P
V_1P05_DSW_INT_RC
C836 1uF X5R_B 0402 6.3 V
TP_PCH_AJ22 TP337
PCH_DCPRTC C1017 16 V 0.1 uF 0402
PCH_DCPSST SC132 16 V 0.1 uF 0402
TP_PCH_AE30 TP338
TP_PCH_P19 TP339
N8/SB
Q87
C1
C2
SR137
None
L
CAD NOTE : PLACE MLCC CLOSE TO PCH
SC44 10uF X5R_B 0805 6.3 V
SC47 1 uF X7R_C 0603/1608 6.3 V
C1016 0.1 uF 0402 16 V
C930 0.1 uF 0402 16 V NI
C931 0.1 uF 0402 16 V
CAD NOTE : PLACE MLCC CLOSE TO PCH T14
+3_3V_DUAL
SC53 1uF X5R_B 0402 6.3 V
SC352 0.1 uF 0402 16 V
CLOSE TO PCH PIN AK20
CLOSE TO PCH PIN AW26
SC530 1uF X5R_B 0402 6.3 V
SC552 0.1 uF 0402 16 V
CLOSE TO PCH PIN AP35
CLOSE TO PCH PIN AN33
+3_3V
SC561 1uF X5R_B 0402 6.3 V
C958 0.1 uF 0402 16 V
CLOSE TO PCH PIN AF26
CLOSE TO PCH PIN AG1
SC559 0.1 uF 0402 16 V
C959 0.1 uF 0402 16 V
CLOSE TO PCH PIN W30
CLOSE TO PCH PIN B6
SC673 1uF X5R_B 0603/1608 6.3 V
SC674 0.1 uF 0402 16 V
SC672 0.1 uF 0402 16 V
CLOSE TO PCH PIN C39
C1050 0.1 uF 0402 16 V
CAD NOTE : PLACE MLCC CLOSE TO PCH AW39
LITE-ON TECHNOLOGY CORP.
Title
21. PCH-9: Power 1
Size C
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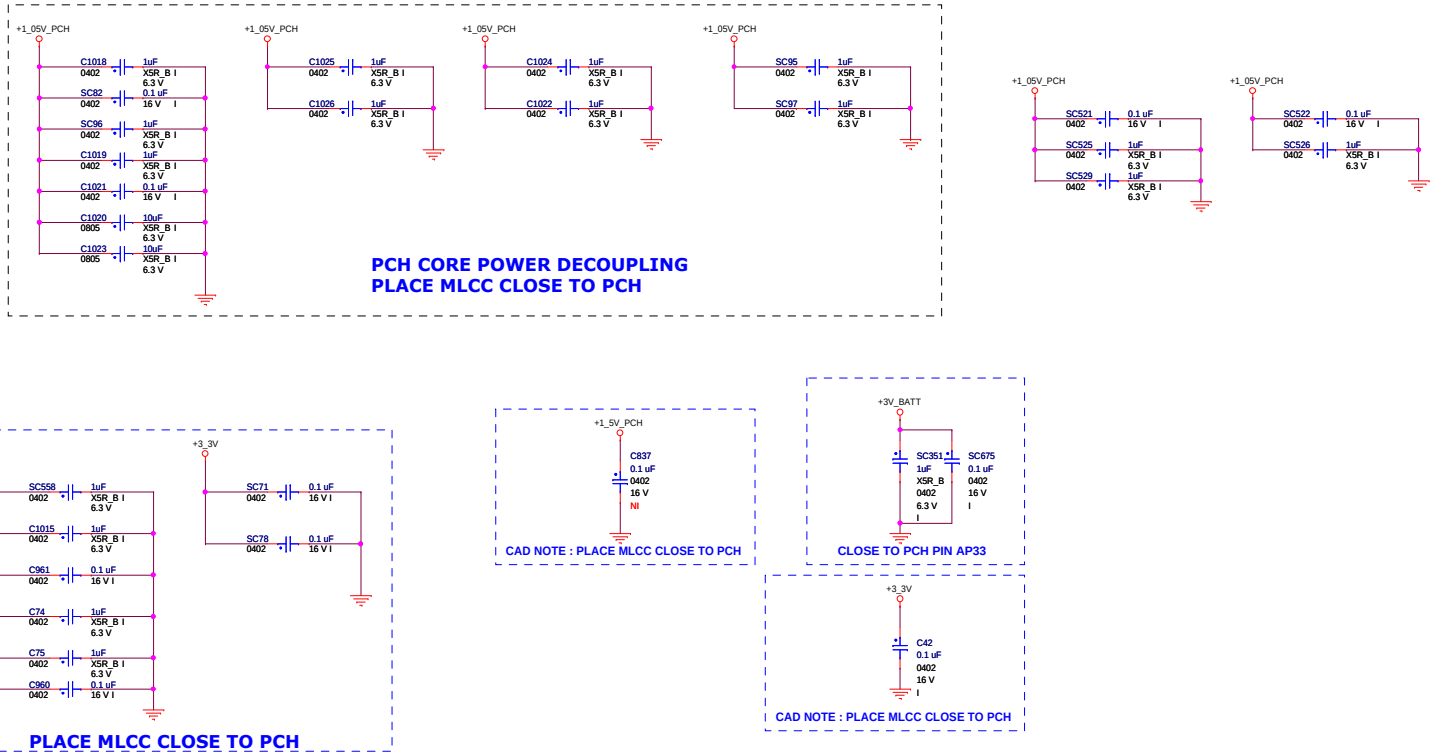

LITE-ON TECHNOLOGY CORP.		LITEON
Title	22. PCH-10: Power 2	
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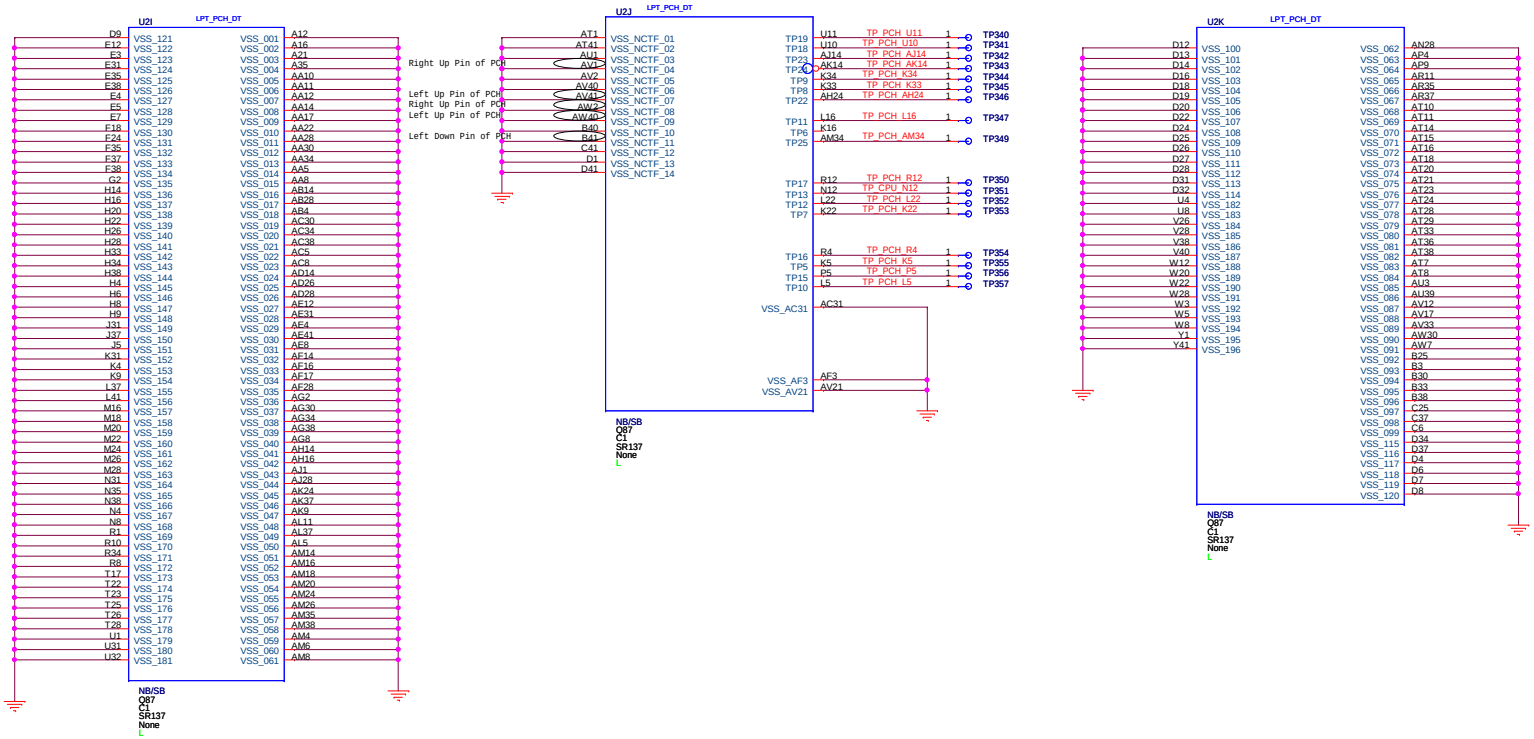

LITE-ON TECHNOLOGY CORP.			
Title	23. PCH-11: GND		
Size C	Document Number JC184/JC186		Rev A01
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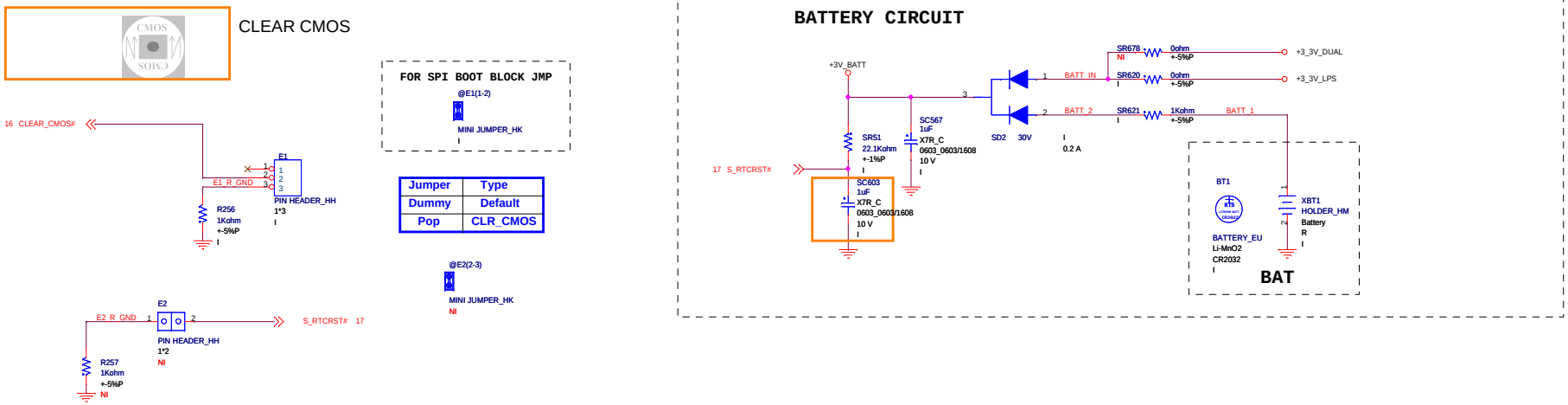

LITE-ON TECHNOLOGY CORP.		
Title: 24. CMOS Clear / Battery		
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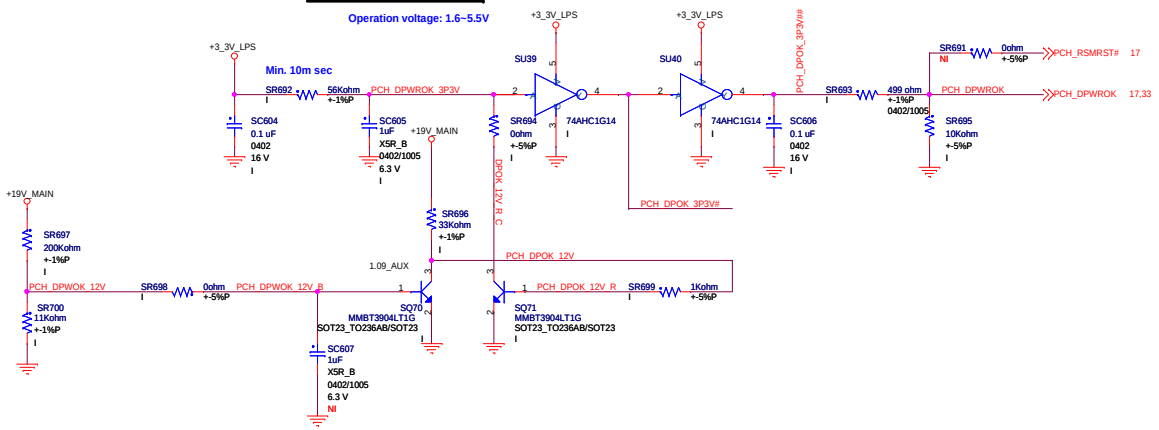
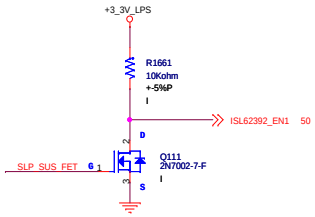
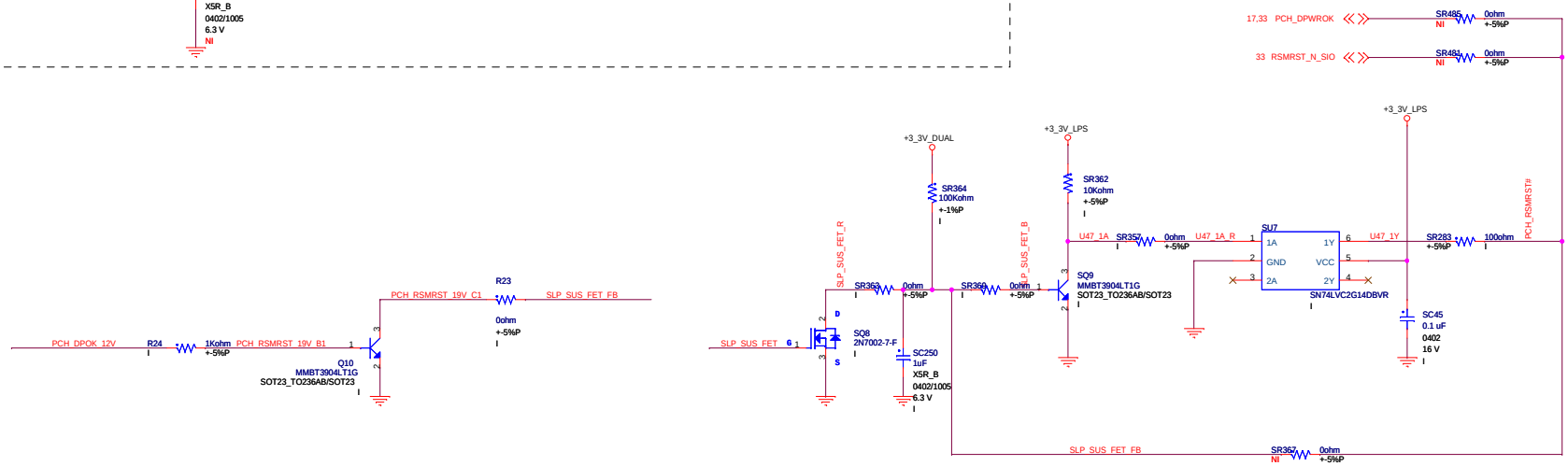
PCH_DPWROK

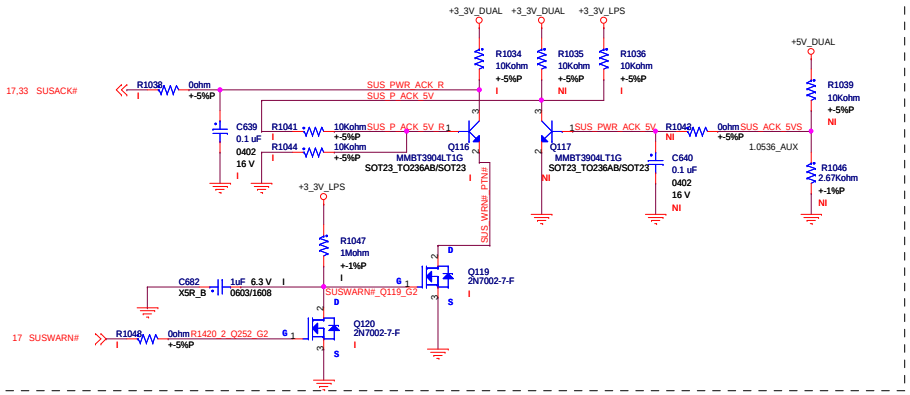
Operation voltage: 1.6~5.5V



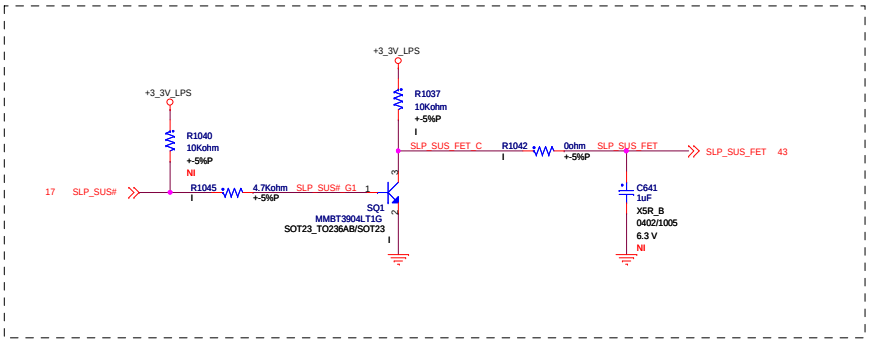




+5V_DUAL SUS ACK



DSW CONTROL SIGNAL



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Title	25. DSW	
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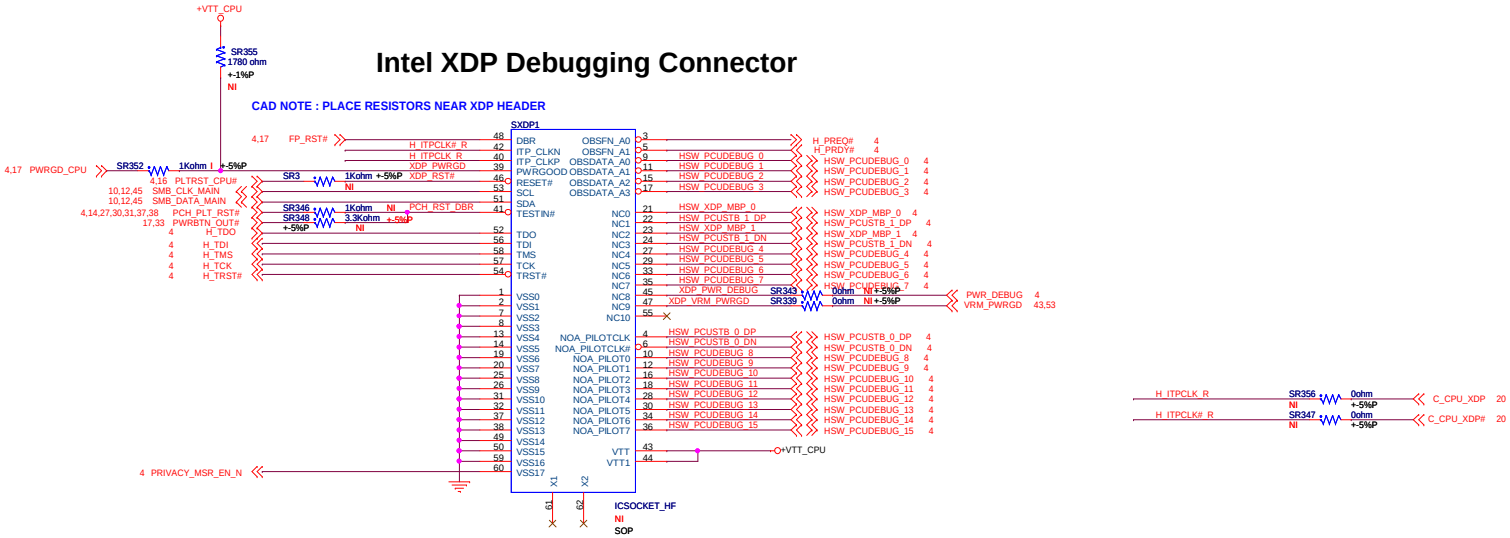
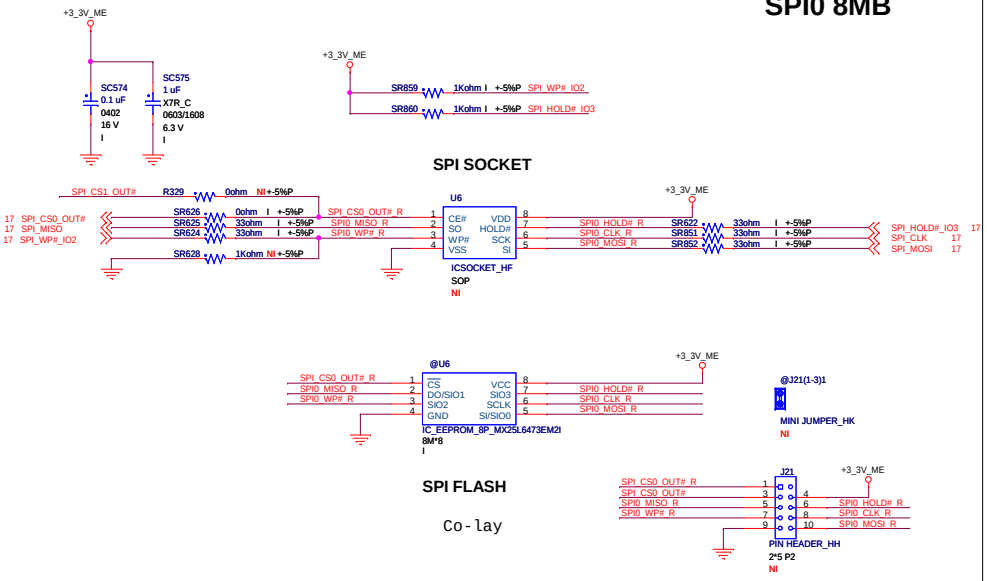
Intel XDP Debugging Connector

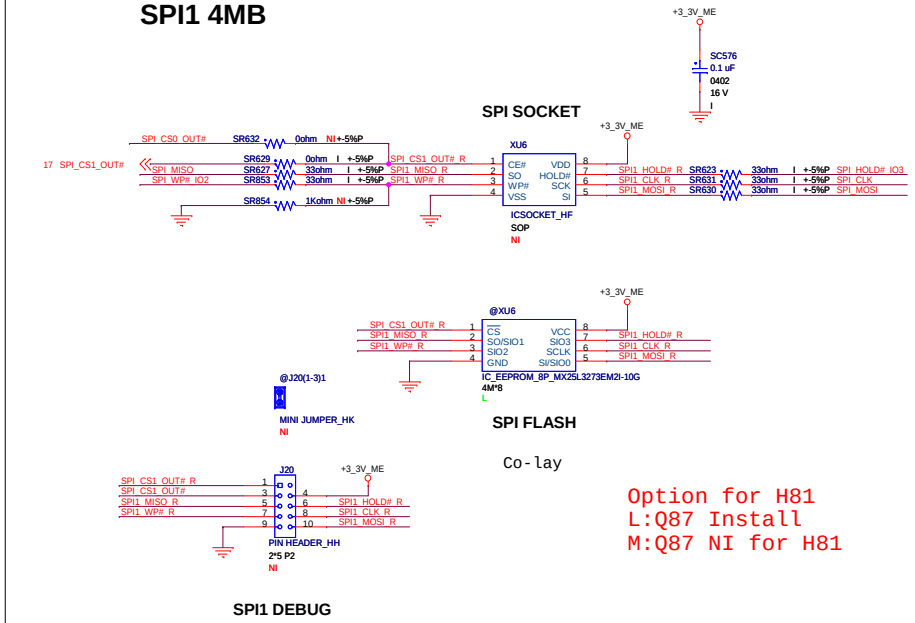
CAD NOTE : PLACE RESISTORS NEAR XDP HEADER



SPI0 8MB

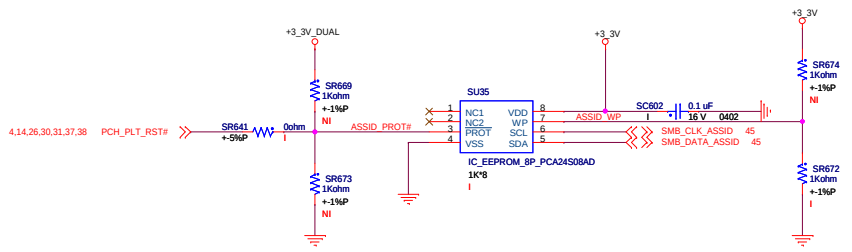


SPI1 4MB



Option for H81
L:Q87 Install
M:Q87 NI for H81

LITE-ON TECHNOLOGY CORP.	LITEON	
Title	26. SPI/XDP	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 26 of 62	

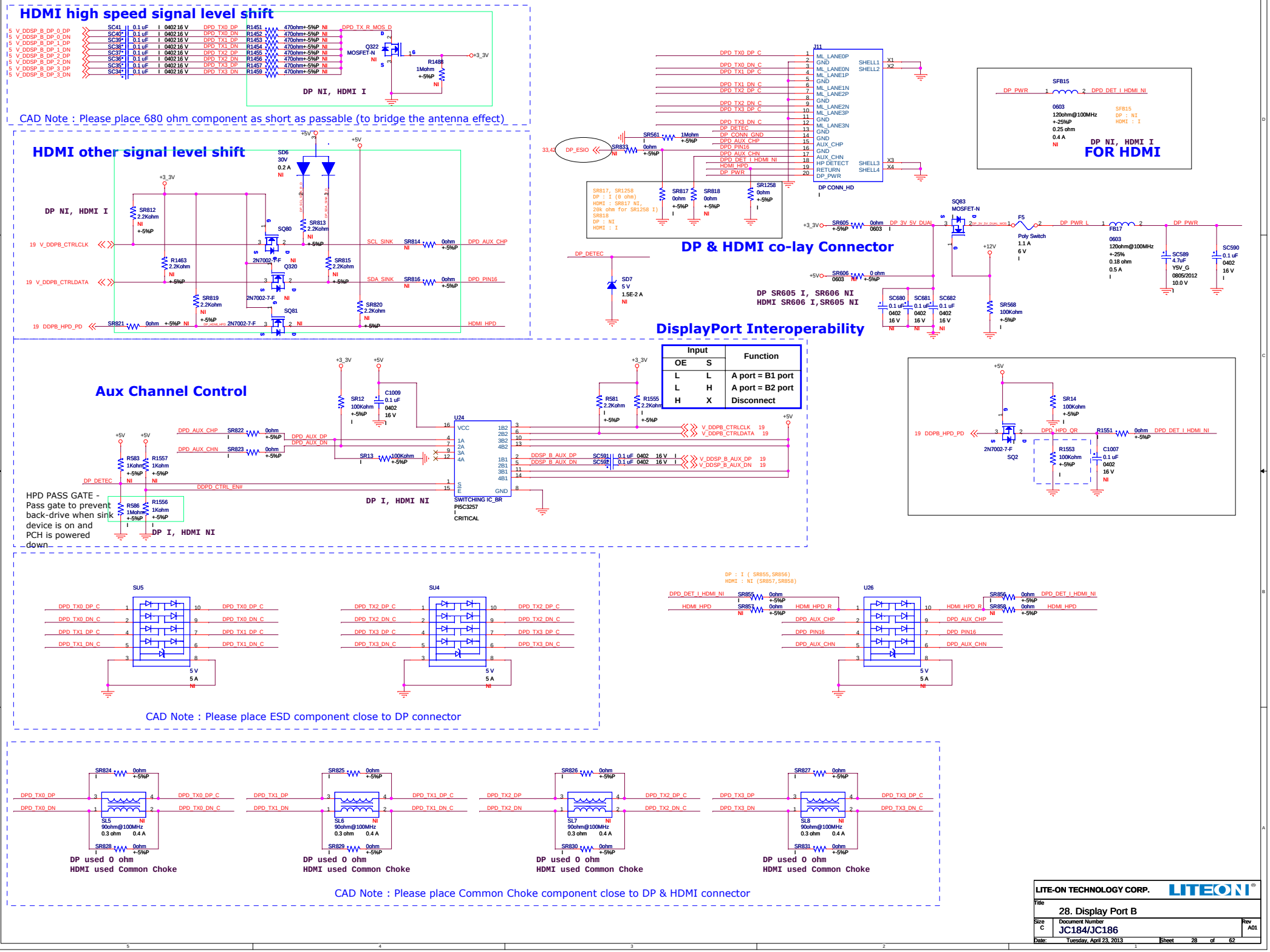


LITE-ON TECHNOLOGY CORP.

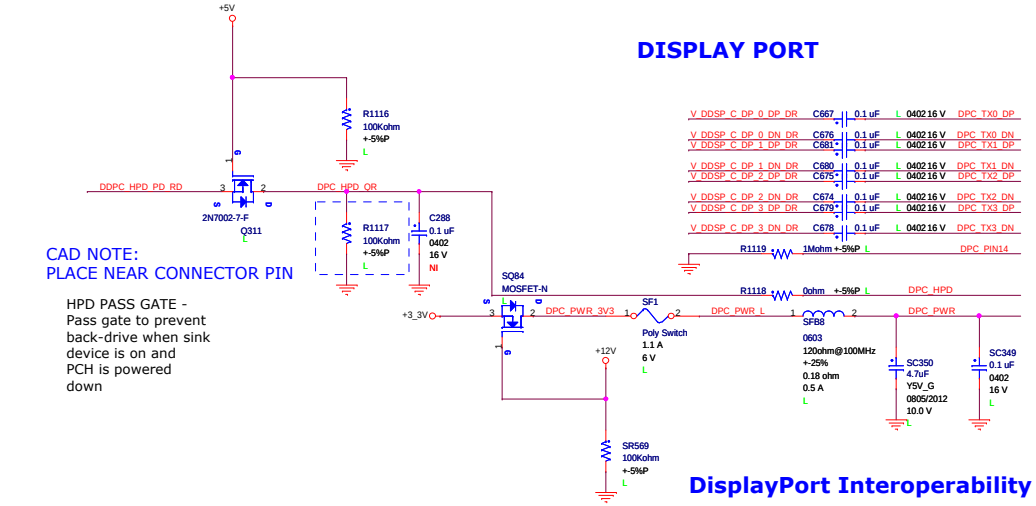
Title: 27. Asset ID - PCA24S08AD

Size: C | Document Number: JC184/JC186 | Rev: A01

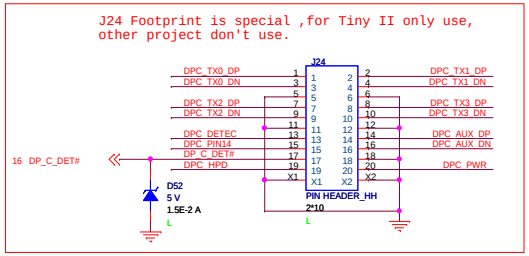
Date: Tuesday, April 23, 2013 | Sheet 27 of 62


HDMI high speed signal level shift
DP NI, HDMI I
CAD Note : Please place 680 ohm component as short as passable (to bridge the antenna effect)
HDMI other signal level shift
DP NI, HDMI I
DP & HDMI co-lay Connector
DP NI, HDMI I
FOR HDMI
DP SR605 I, SR606 NI
HDMI SR606 I,SR605 NI
DisplayPort Interoperability
Aux Channel Control
HPD PASS GATE -
Pass gate to prevent back-drive when sink device is on and PCH is powered down
DP I, HDMI NI
DP I, HDMI NI
SWITCHING IC_BR
PI5C3257
CRITICAL
CAD Note : Please place ESD component close to DP connector
DP used 0 ohm
HDMI used Common Choke
DP used 0 ohm
HDMI used Common Choke
DP used 0 ohm
HDMI used Common Choke
DP used 0 ohm
HDMI used Common Choke
CAD Note : Please place Common Choke component close to DP & HDMI connector
LITE-ON TECHNOLOGY CORP.
Title
28. Display Port B
Size C
Document Number
JC184/JC186
Rev A01
Date: Tuesday, April 23, 2013
Sheet 28 of 62

DISPLAY PORT

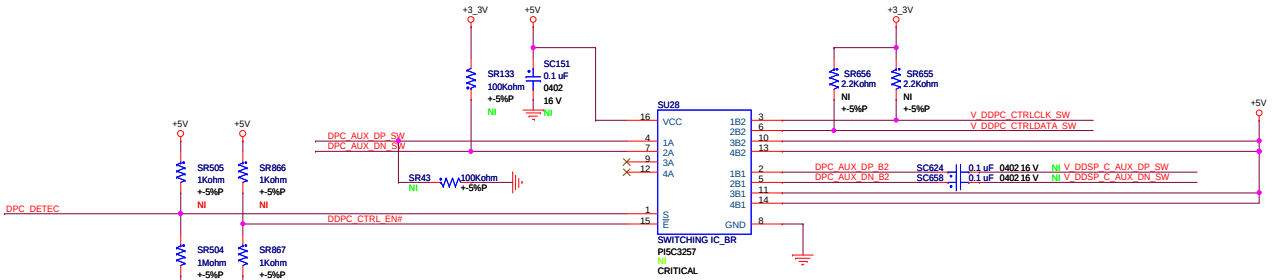


DisplayPort Interoperability

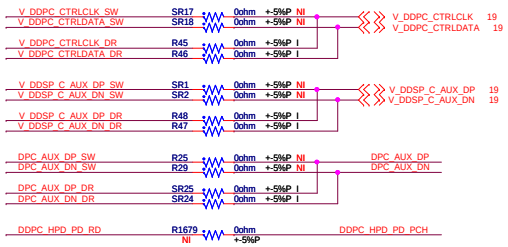


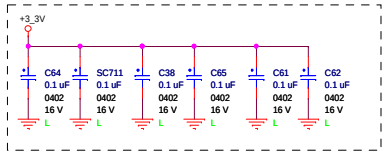
On Cable side Pin17 & Pin 18 need short

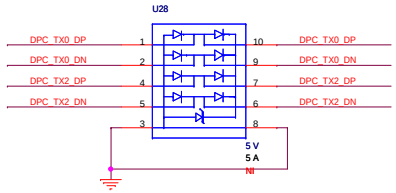
DPC_DETEC
L : Connect to Display Port or No Connection
H : Connect to Doungle

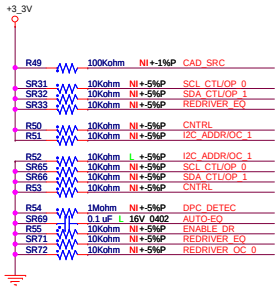


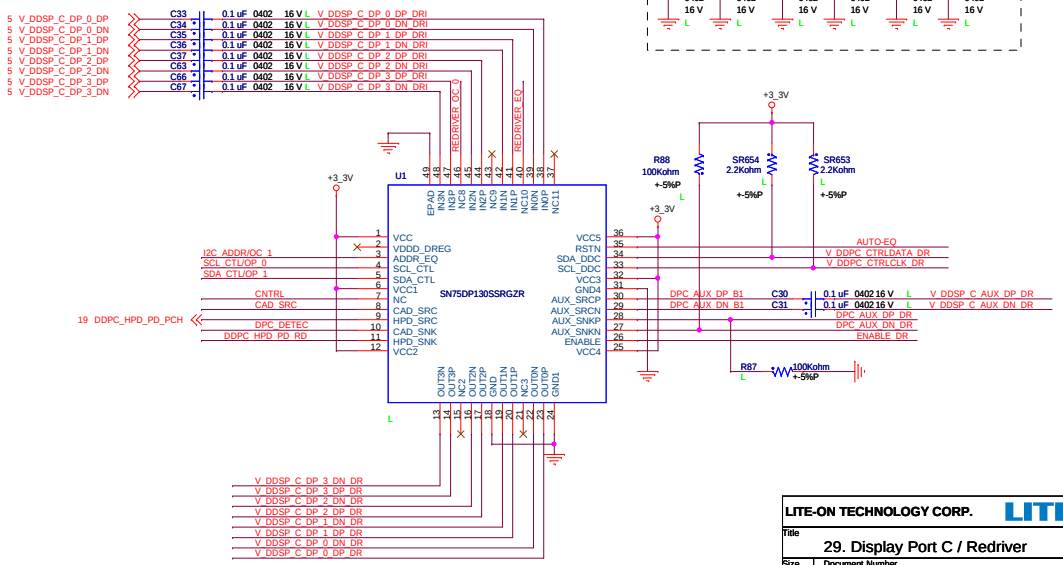
Input		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

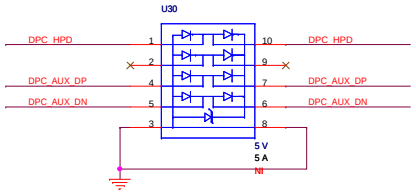


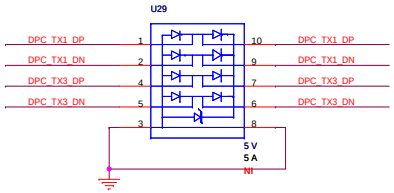






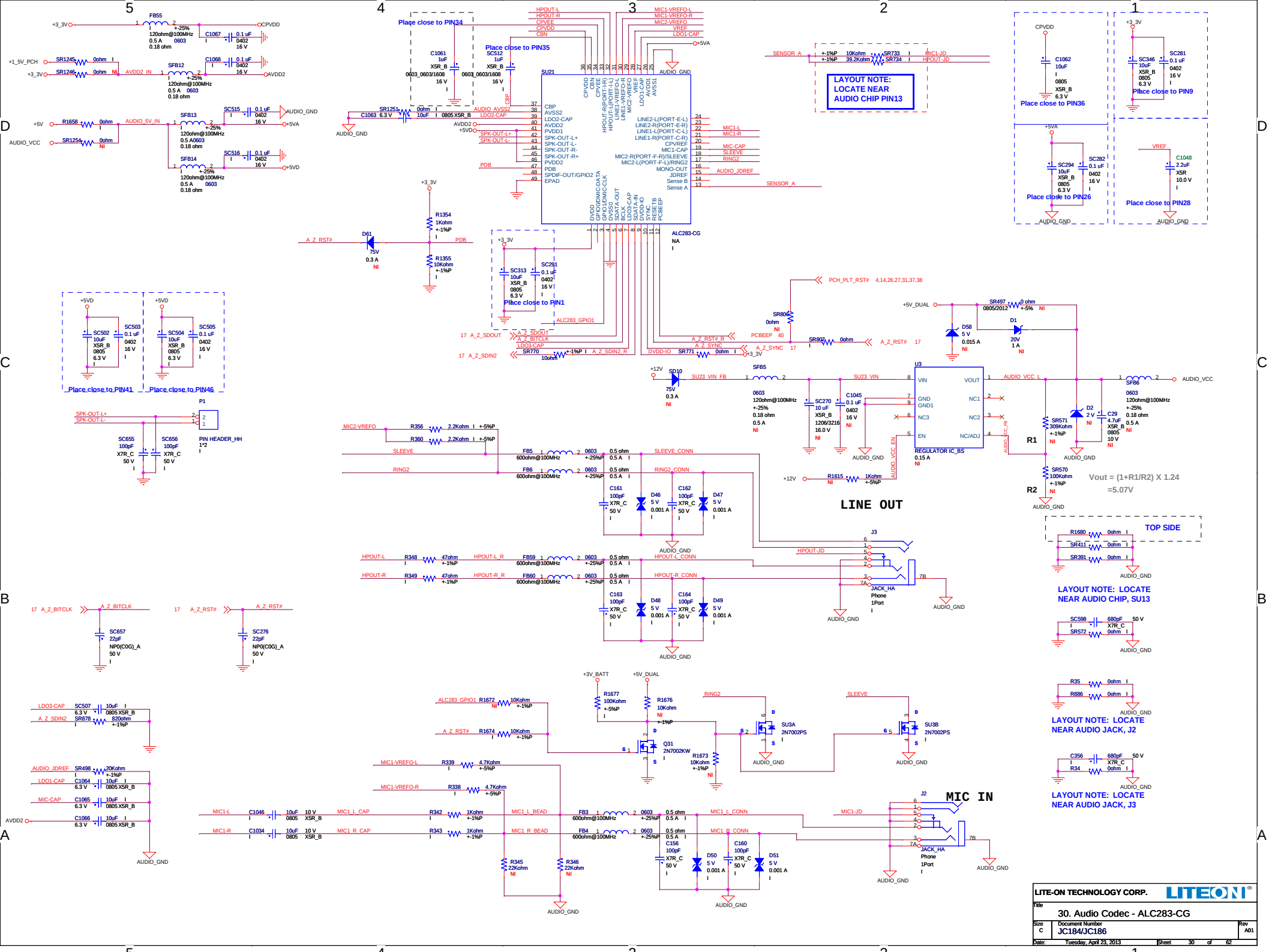


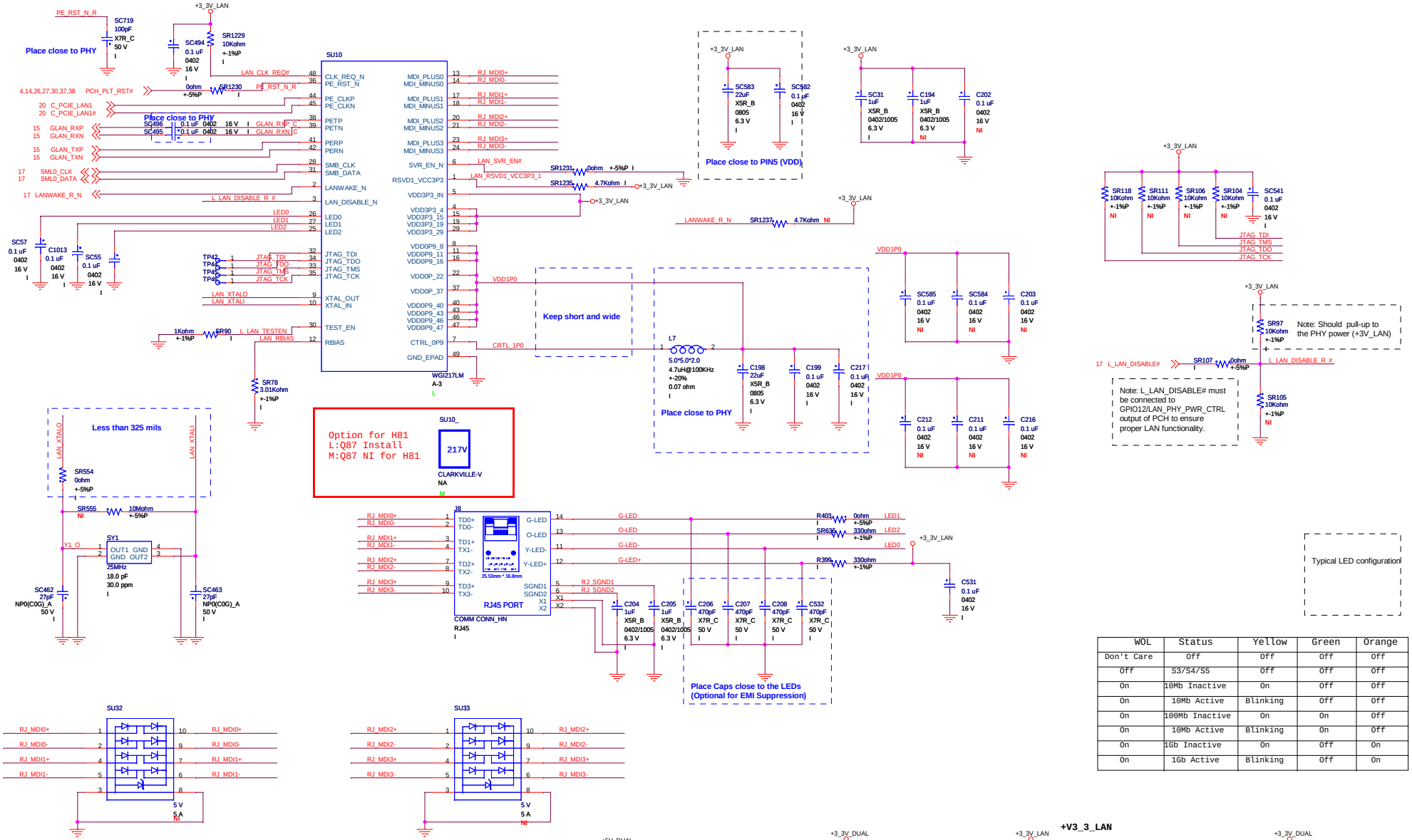




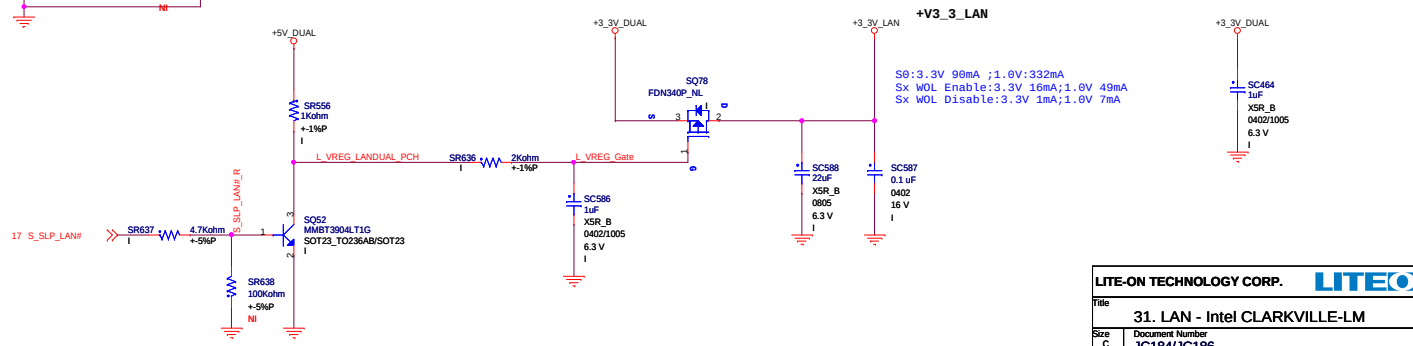
CAD Note : Please place ESD component close to DP connector

LITE-ON TECHNOLOGY CORP.		LITEON
Title	29. Display Port C / Redriver	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 29 of 62	


SU21
ALC283-CG
LINE OUT
MIC IN
LAYOUT NOTE: LOCATE NEAR AUDIO CHIP PIN13
Place close to PIN34
Place close to PIN35
Place close to PIN36
Place close to PIN9
Place close to PIN26
Place close to PIN28
Place close to PIN1
Place close to PIN41
Place close to PIN46
TOP SIDE
LAYOUT NOTE: LOCATE NEAR AUDIO CHIP, SU13
LAYOUT NOTE: LOCATE NEAR AUDIO JACK, J2
LAYOUT NOTE: LOCATE NEAR AUDIO JACK, J3
Vout = (1+R1/R2) X 1.24
=5.07V
LITE-ON TECHNOLOGY CORP.
30. Audio Codec - ALC283-CG
JC184/JC186
Tuesday, April 23, 2013



WOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off
Off	S3/S4/S5	Off	Off	Off
On	10Mb Inactive	On	Off	Off
On	10Mb Active	Blinking	Off	Off
On	100Mb Inactive	On	On	Off
On	10Mb Active	Blinking	On	Off
On	1Gb Inactive	On	Off	On
On	1Gb Active	Blinking	Off	On



LITE-ON TECHNOLOGY CORP.

Title: 31. LAN - Intel CLARKVILLE-LM

Size: C | Document Number: JC184/JC186 | Rev: A01

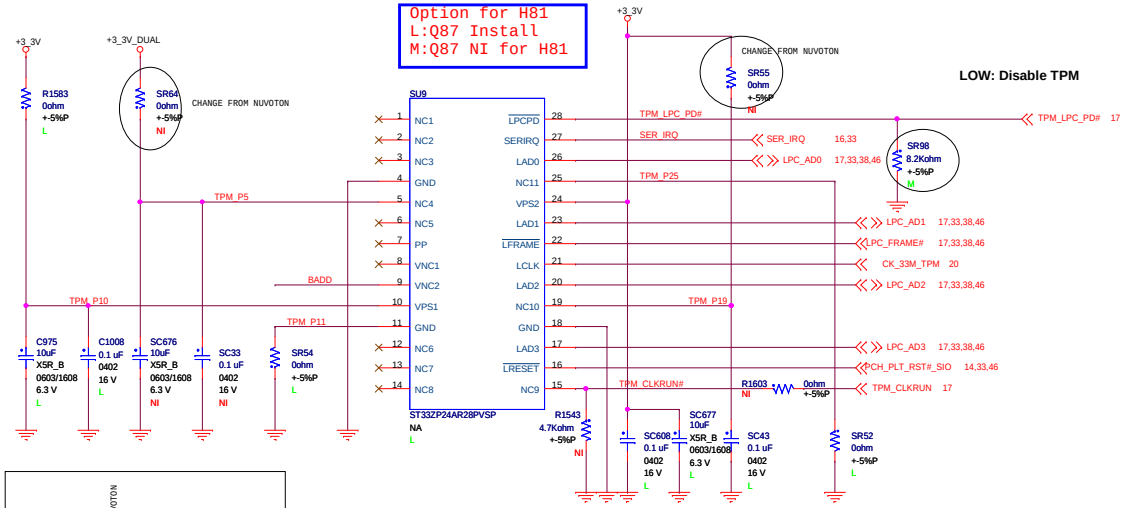
Date: Tuesday, April 23, 2013 | Sheet 31 of 62

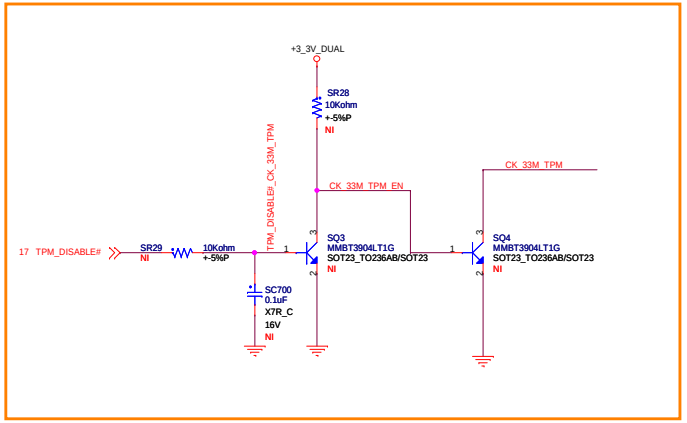
NUVOTON:
SR64,SC676,SC33,SR55-->I
R1583,C975,C1008,SR54-->NI

ST:
SR64,SC676,SC33,SR55-->NI
R1583,C975,C1008,SR54-->I

TPM

Option for H81
L:Q87 Install
M:Q87 NI for H81



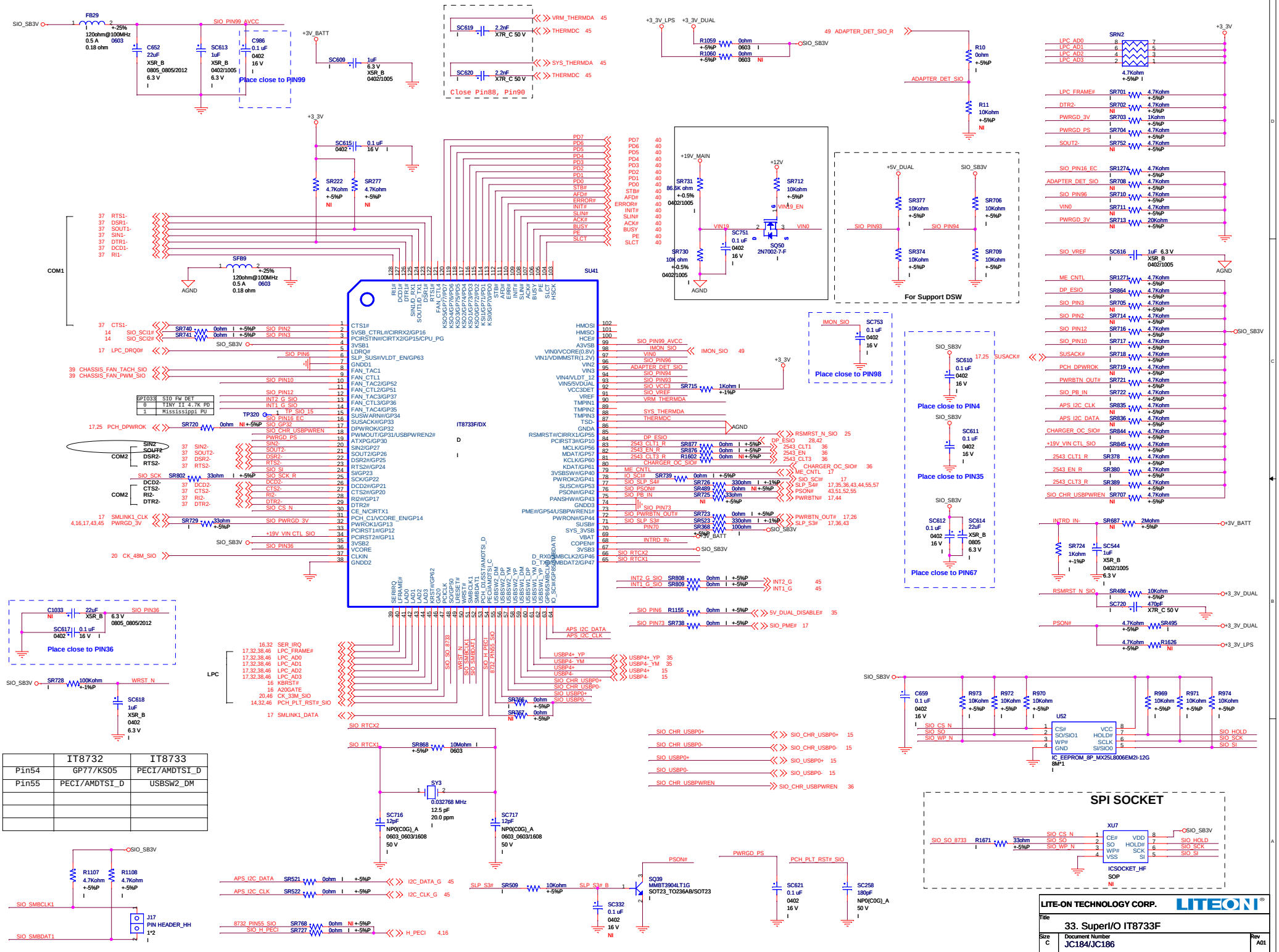


BADD	SELECTION
0	EEh - EFh
1	7Eh - 7Fh

' 1 ' - Pin is left open.
' 0 ' - pin is pulled down.

Base Address
EE / EF

LITE-ON TECHNOLOGY CORP.		LITEON
Title	32. TPM - ST ST33ZP24AR28PVSH	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 32 of 62	



	IT8732	IT8733
Pin54	GP77/KS05	PECI/AMDTSI_D
Pin55	PECI/AMDTSI_D	USBSW2_DM

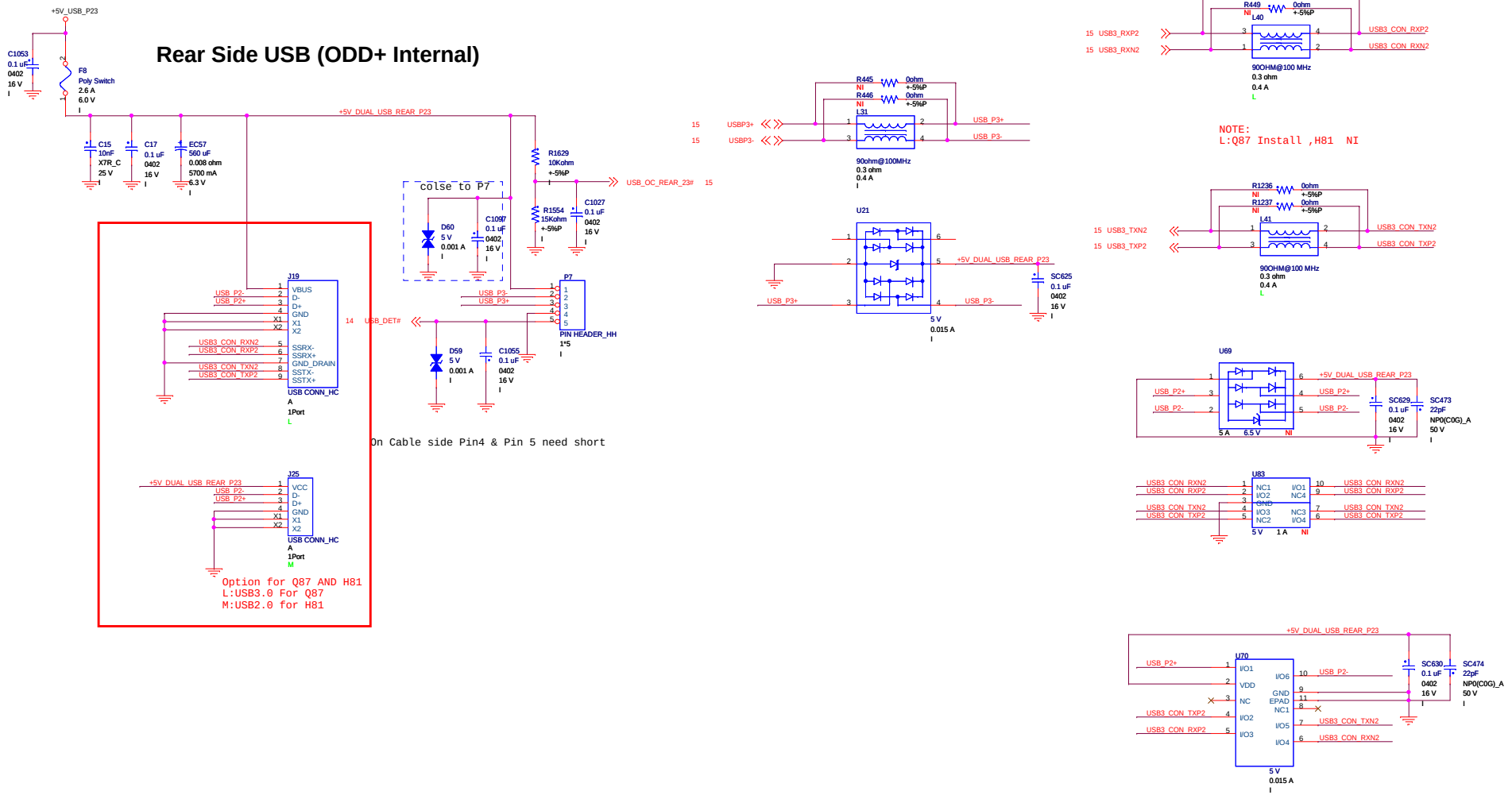
LITE-ON TECHNOLOGY CORP.

Title: 33. SuperI/O IT8733F

Size: C | Document Number: JC184/JC186 | Rev: A01

Date: Tuesday, April 23, 2013 | Sheet 33 of 62

Rear Side USB (ODD+ Internal)



LITE-ON TECHNOLOGY CORP.		LITEON
Title	34. USB3.0 ODD CONN / Int USB	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 34 of 62	

Rear Side USBx2

NOTE:
Option for Q87 AND H81
L:USB3.0 For Q87
M:USB2.0 For H81

NOTE:
L:Q87 Install ,H81 NI

Co-layout

Co-layout

Front Side USBx1

5V_DUAL_DISABLE#	H	H	L	L
SLP_S4#	H	L	H	L
+5V_USB_P4_EN	H	H	H	L

Discharge

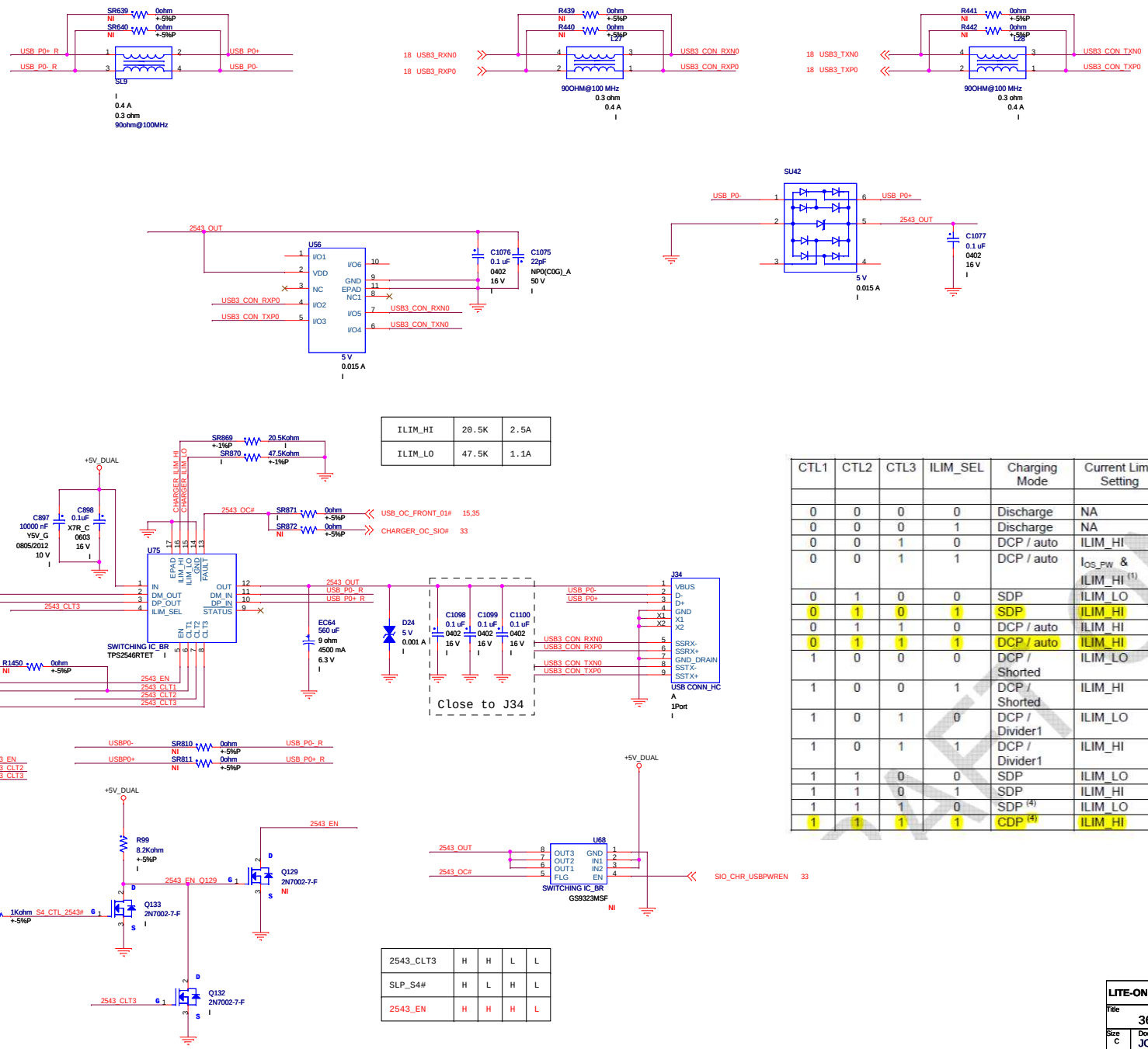
LITE-ON TECHNOLOGY CORP. LITEON

Title: 35. USB3.0 CONN x 3

Size: C | Document Number: JC184/JC186 | Rev: A01

Date: Tuesday, April 23, 2013 | Sheet 35 of 62

FRONT USB3.0 Charger x 1



ILIM_HI	20.5K	2.5A
ILIM_LO	47.5K	1.1A

CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
						off
0	0	0	0	Discharge	NA	off
0	0	0	1	Discharge	NA	off
0	0	1	0	DCP / auto	ILIM_HI	off
0	0	1	1	DCP / auto	I_{OS_PW} & ILIM_HI (1)	DCP load present (2)
0	1	0	0	SDP	ILIM_LO	off
0	1	0	1	SDP	ILIM_HI	off
0	1	1	0	DCP / auto	ILIM_HI	off
0	1	1	1	DCP / auto	ILIM_HI	DCP load present (3)
1	0	0	0	DCP / Shorted	ILIM_LO	off
1	0	0	1	DCP / Shorted	ILIM_HI	off
1	0	1	0	DCP / Divider1	ILIM_LO	off
1	0	1	1	DCP / Divider1	ILIM_HI	off
1	1	0	0	SDP	ILIM_LO	off
1	1	0	1	SDP	ILIM_HI	off
1	1	1	0	SDP (4)	ILIM_LO	off
1	1	1	1	CDP (4)	ILIM_HI	CDP load present (5)

2543_CLT3	H	H	L	L
SLP_S4#	H	L	H	L
2543_EN	H	H	H	L

AFTER ONLY

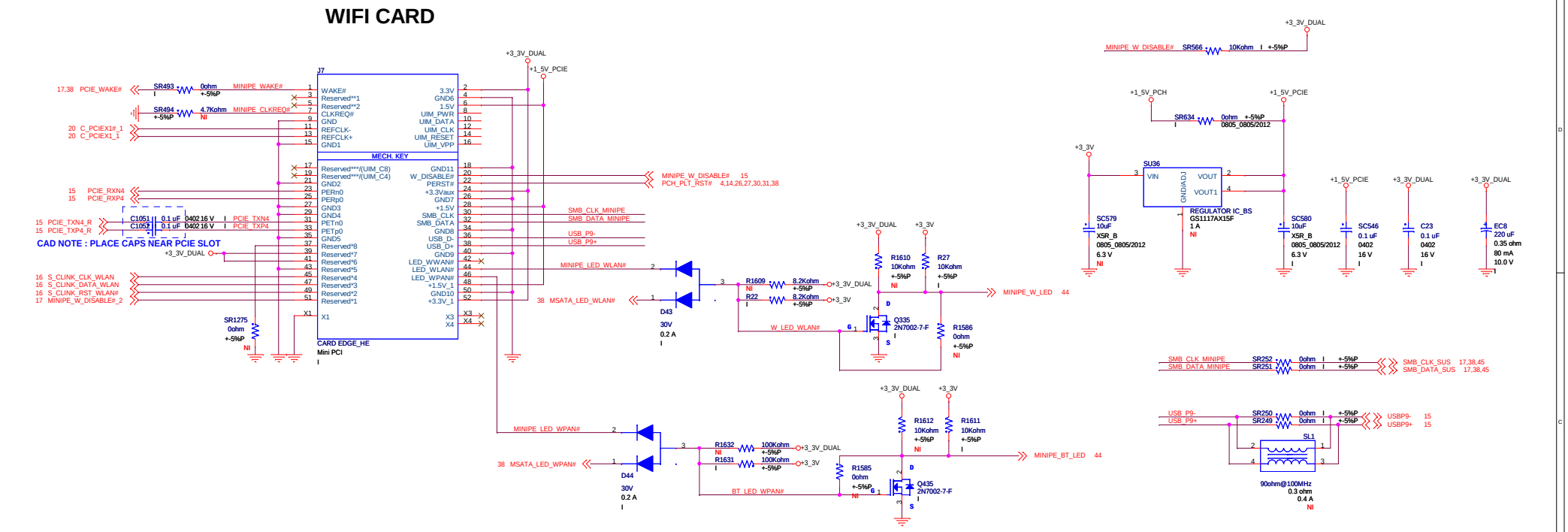
LITE-ON TECHNOLOGY CORP.

Title: 36. USB3.0 x1/ USB CHARGER

Size: C | Document Number: JC184/JC186 | Rev: A01

Date: Tuesday, April 23, 2013 | Sheet 36 of 62

WIFI CARD

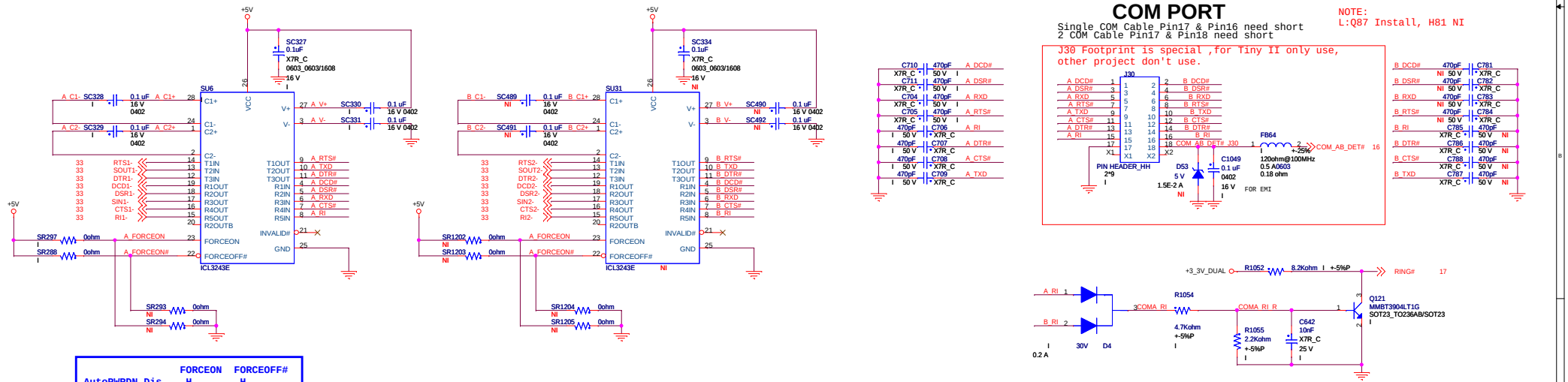


COM PORT

Single COM Cable Pin17 & Pin16 need short
2 COM Cable Pin17 & Pin18 need short

NOTE:
L:Q87 Install, H81 NI

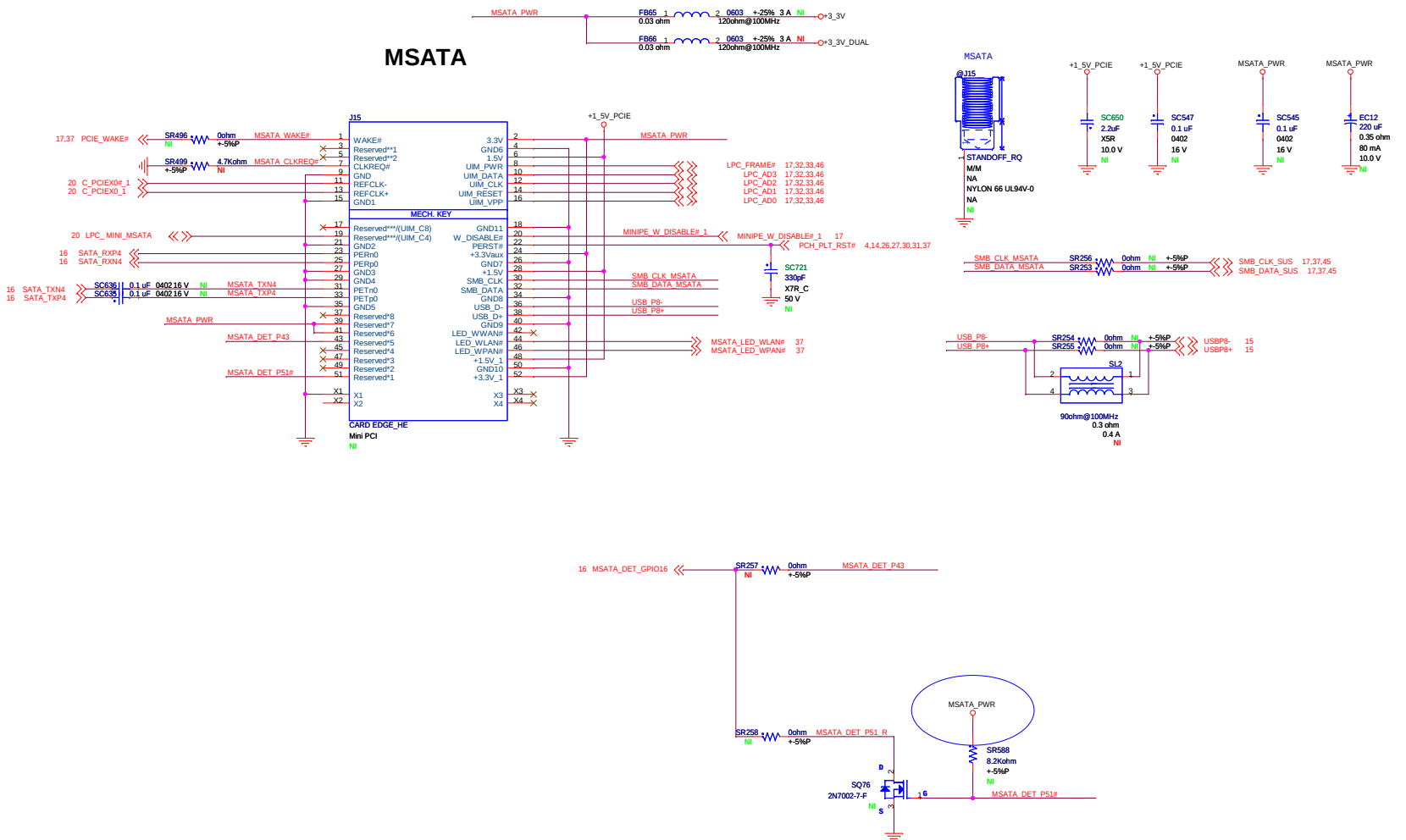
J30 Footprint is special ,for Tiny II only use, other project don't use.



	FORCEON	FORCEOFF#
AutoPWRDN Dis	H	H
AutoPWRDN En	L	H

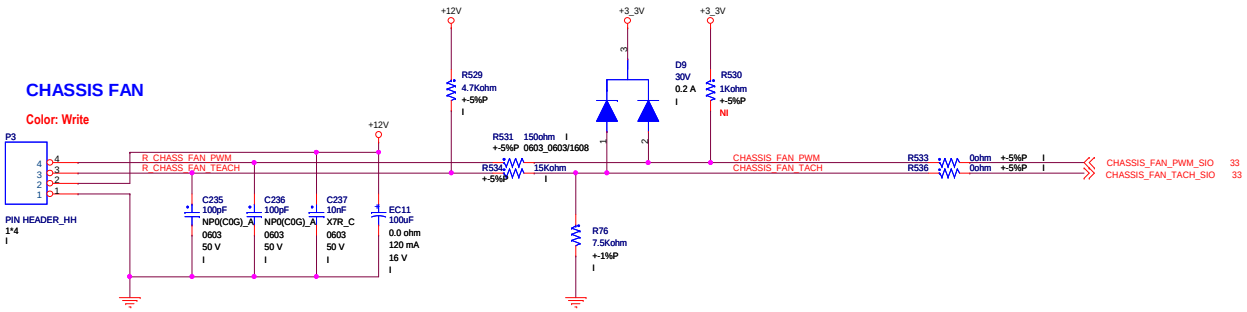
LITE-ON TECHNOLOGY CORP.	LITEON
Title	37. Mini PCIE WiFi / 2 COM PORT
Size C	Document Number JC184/JC186
Rev	A01
Date: Tuesday, April 23, 2013	Sheet 37 of 62

MSATA

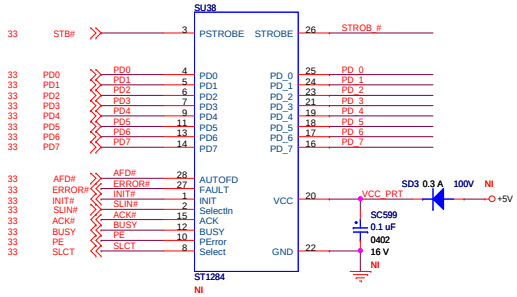


LITE-ON TECHNOLOGY CORP.		LITEON
Title	38. MSATA	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 38 of 62	

CHASSIS/CPU/PSU FAN

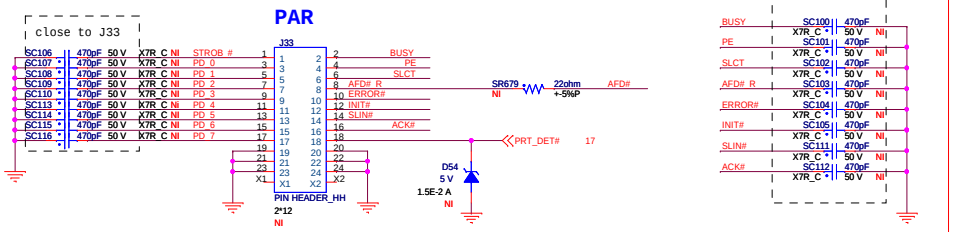


LITE-ON TECHNOLOGY CORP.		LITEON
Title	39. FAN CRTL	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 39 of 62	

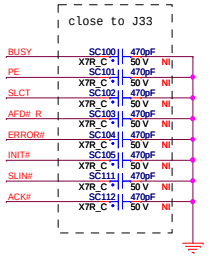


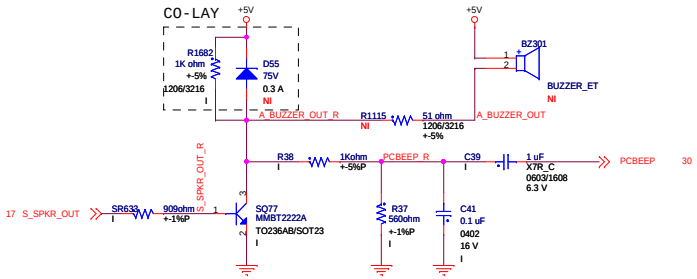
PARALLEL PORT

NOTE:
L:Q87 Install, H81 NI



J33 Footprint is special ,for Tiny II only use,
other project don't use.





LITE-ON TECHNOLOGY CORP.		LITEON
Title	40. Buzzer/Parallel Port/BATT	
Size C	Document Number JC184/JC186	Rev A01
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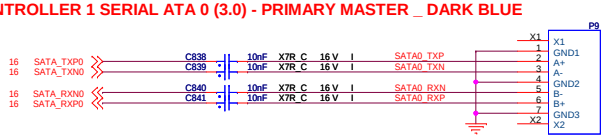
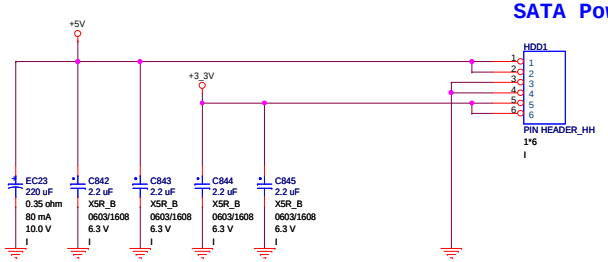
SATA SATA0

CONTROLLER 1 SERIAL ATA 0 (3.0) - PRIMARY MASTER _ DARK BLUE

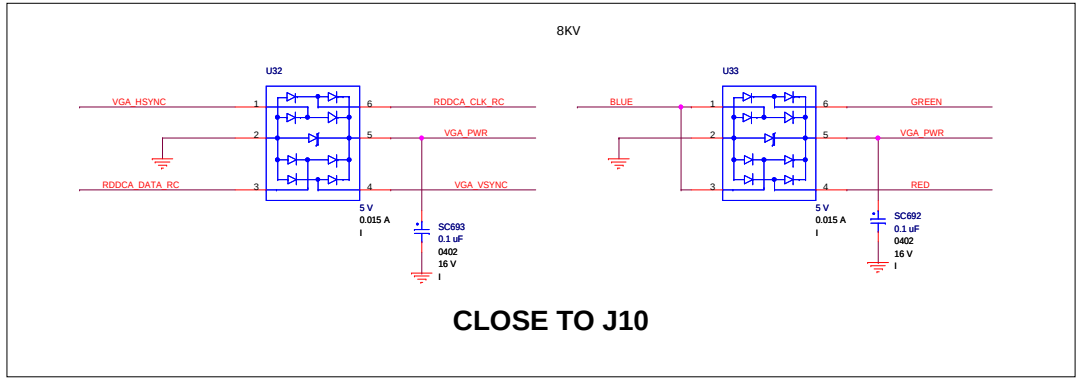


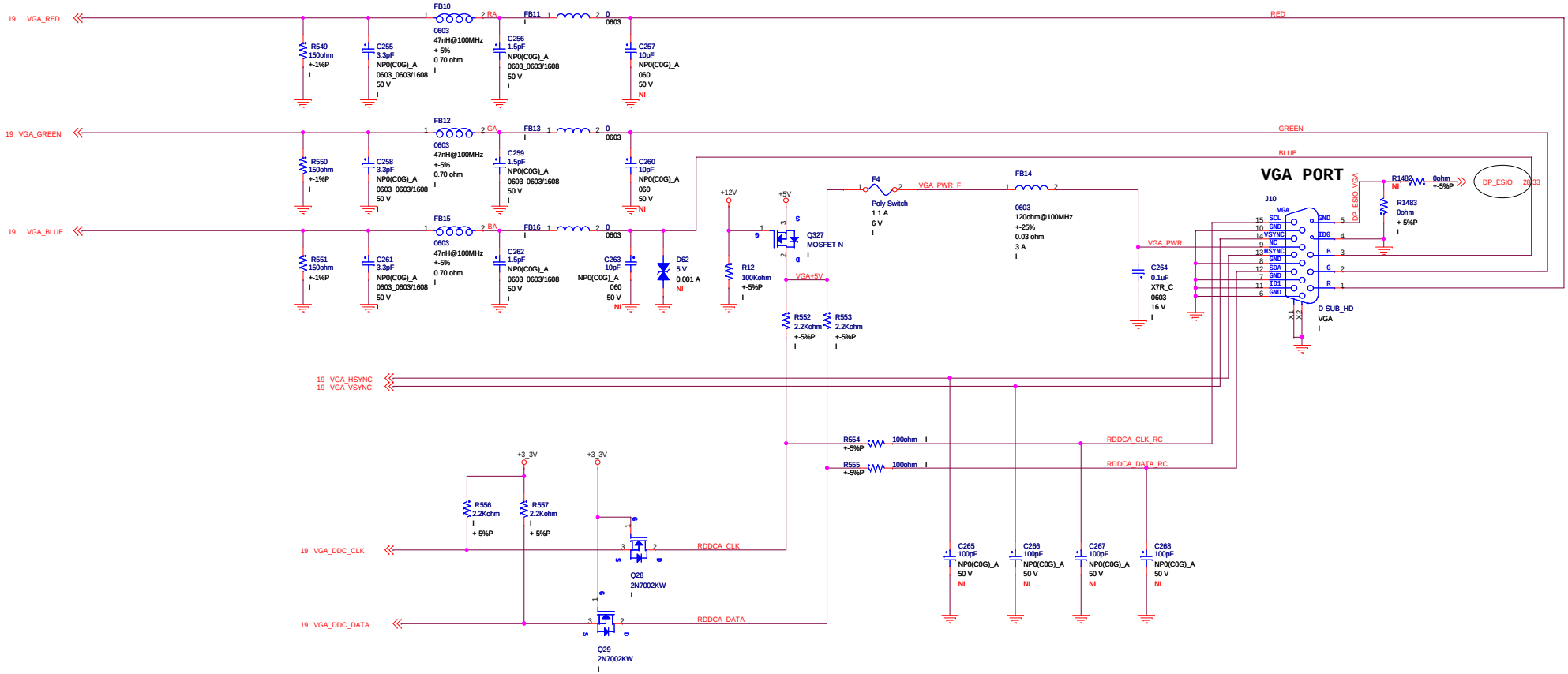
CAD NOTE : PLACE ALL CAPS WITHIN 0.5 INCH OF CONNECTOR

SATA Power



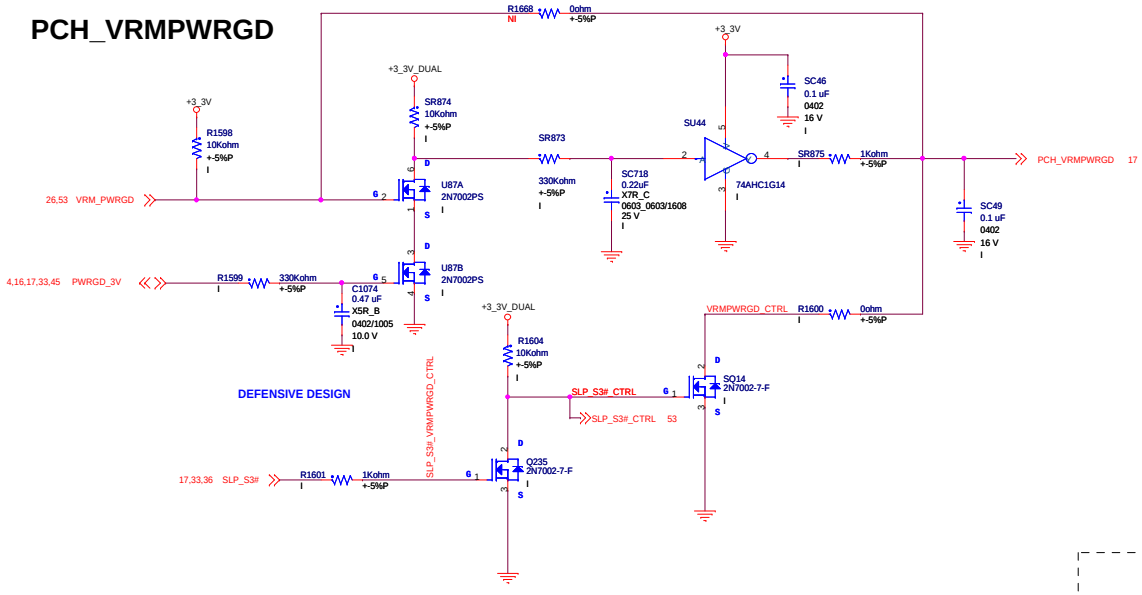
LITE-ON TECHNOLOGY CORP.		LITEON
Title	41. SATA HDD	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 41 of 62	

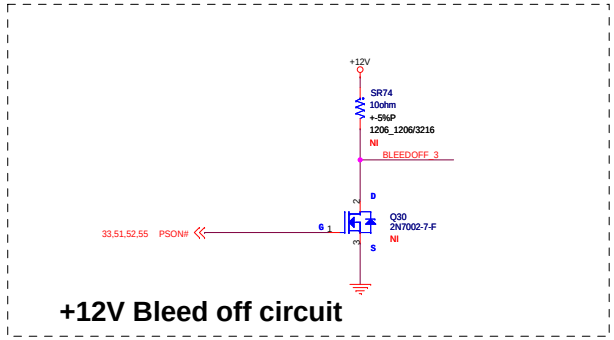




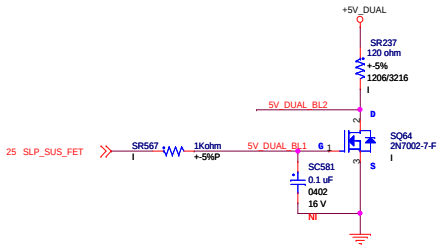
LITE-ON TECHNOLOGY CORP.		LITEON
Title	42. VGA	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 42 of 62	

PCH_VRMPWRGD

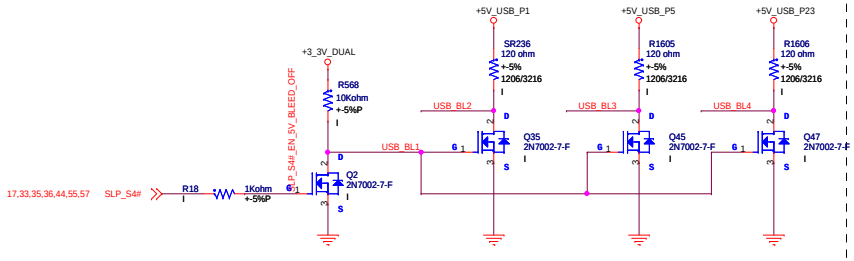




+12V Bleed off circuit

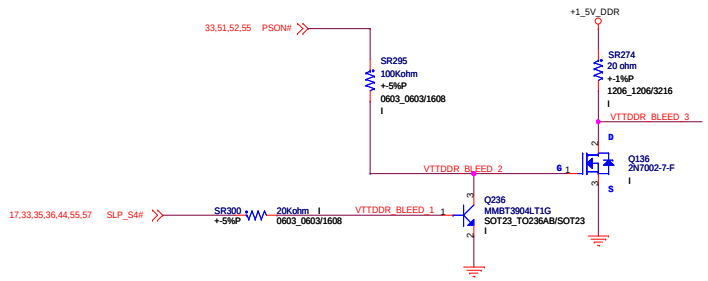


5V_DUAL Bleed off circuit

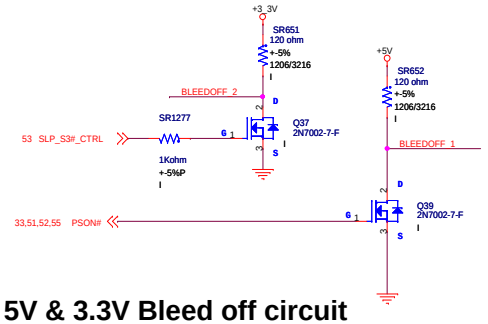


5V_USB Bleed off circuit

DESIGN NOTE:THESE CIRCUITS ARE USED TO BLEED OFF 1.5V DDR



+1_5V_DDR Bleed off circuit



5V & 3.3V Bleed off circuit

LITE-ON TECHNOLOGY CORP.		LITEON
Title	43. PWRGD & BLEED OFF	
Size C	Document Number JC184/JC186	Rev A01
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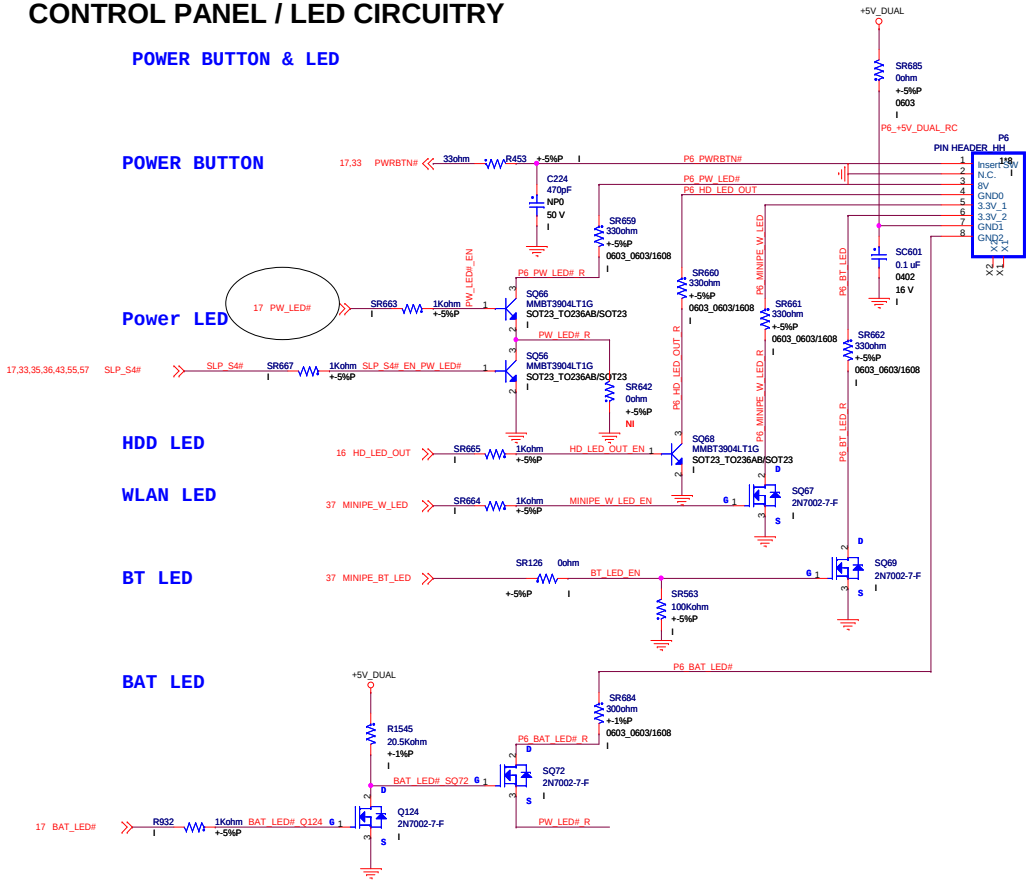
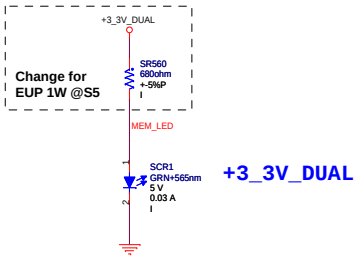
CONTROL PANEL / LED CIRCUITRY



P6 HEADER	Color	Functoin
3 PIN	G	PWR
4 PIN	G	HDD
5 PIN	G	WiFi
6 PIN	G	BT

Id = 25mA @ 2.8V (SPEC)
Id = (5V-2.8V) / 100ohm = 22mA
0.1W (For Current limit R)



PCA LED CIRCUITS

ALL PARTS ON THIS SHEET ARE NI FOR PRODUCTION.

LITE-ON TECHNOLOGY CORP.		LITEON
Title: 44. Button/LED		
Size: C	Document Number: JC184/JC186	Rev: A01
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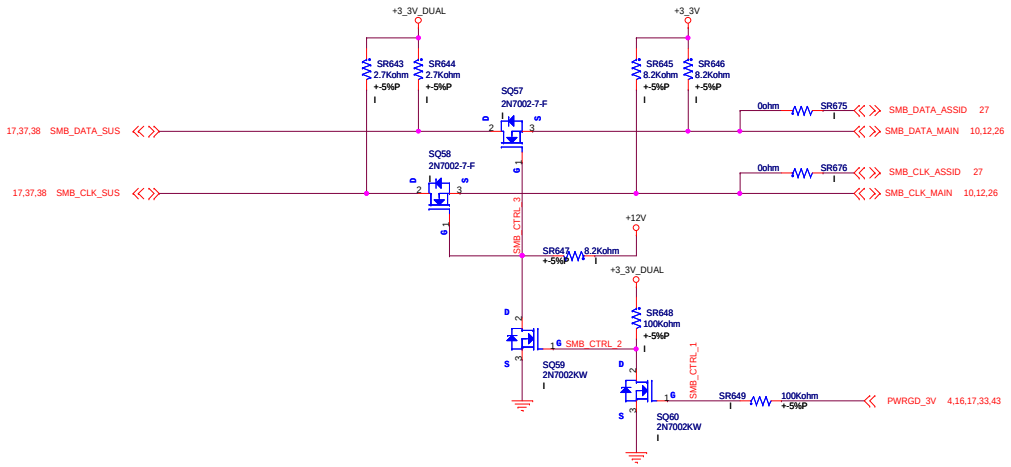
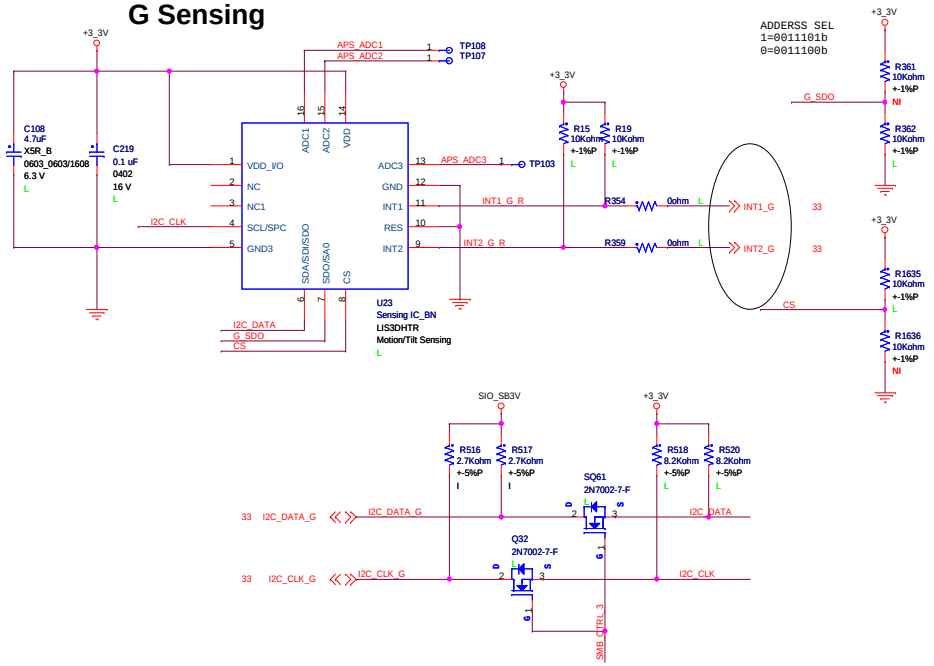
SM Bus

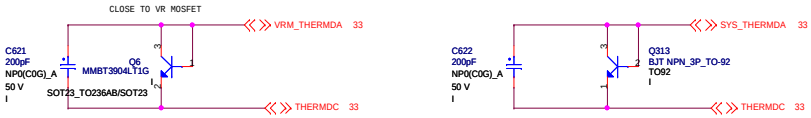


G Sensing



Temperature Sensing

Current Mode

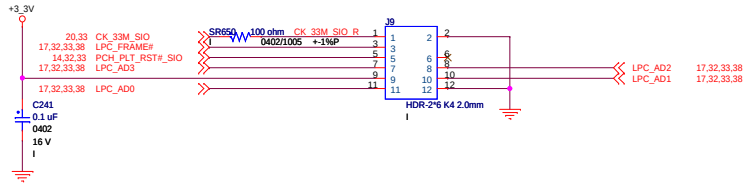


CAD NOTE : Place MLCC Close to Thermal Diode

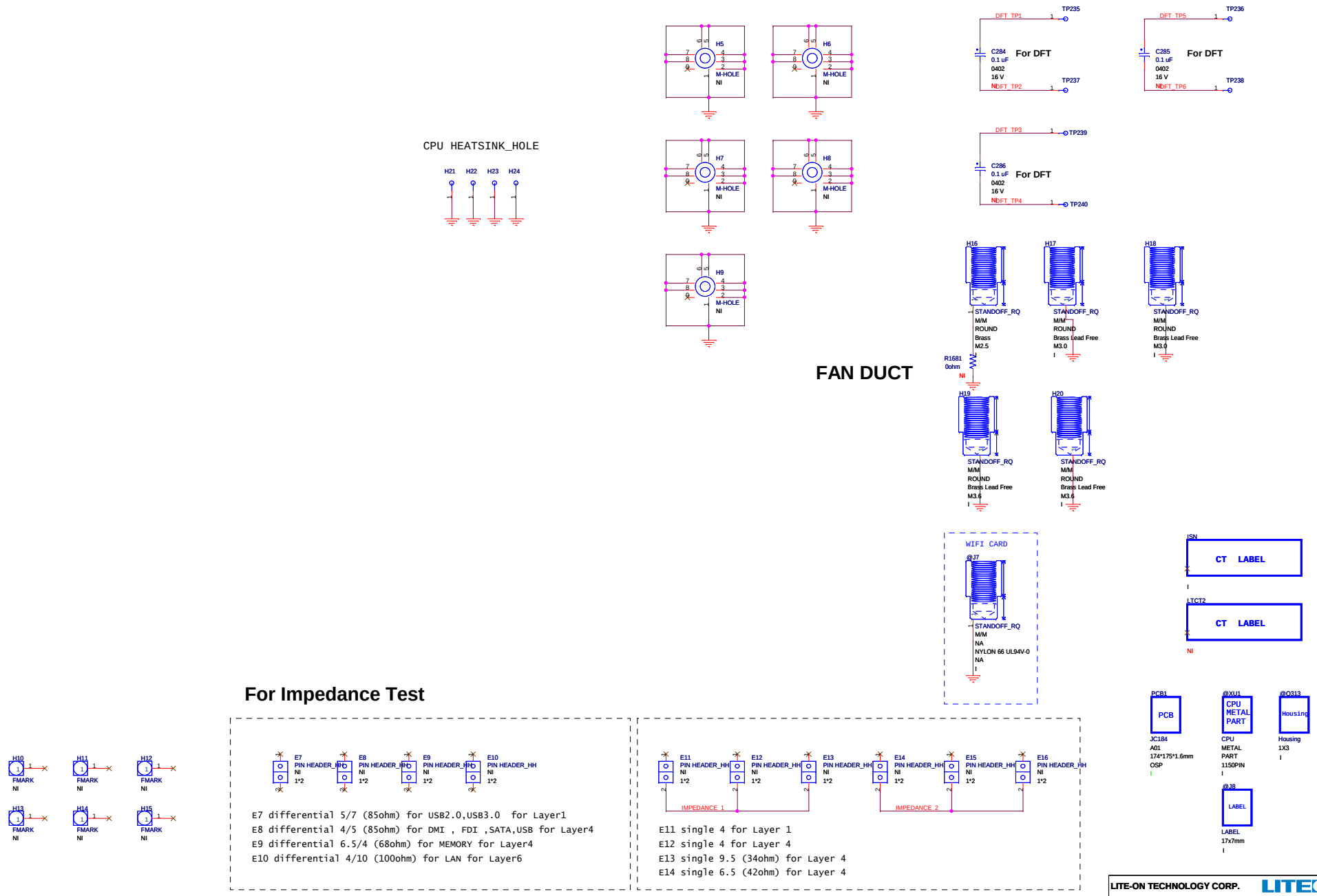
Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconsuctor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

LITE-ON TECHNOLOGY CORP.		LITEON
Title	45. SM BUS/Thermal Sensing/APS	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 45 of 62	

Debug port



LITE-ON TECHNOLOGY CORP.		LITEON
Title	46. Debug Port	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 46 of 62	



LITE-ON TECHNOLOGY CORP.

Title: 47. Mounting Hole

Size: C | Document Number: JC184/JC186 | Rev: A01

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LITE-ON TECHNOLOGY CORP.

Title

48. Blank

Size	Document Number	Rev
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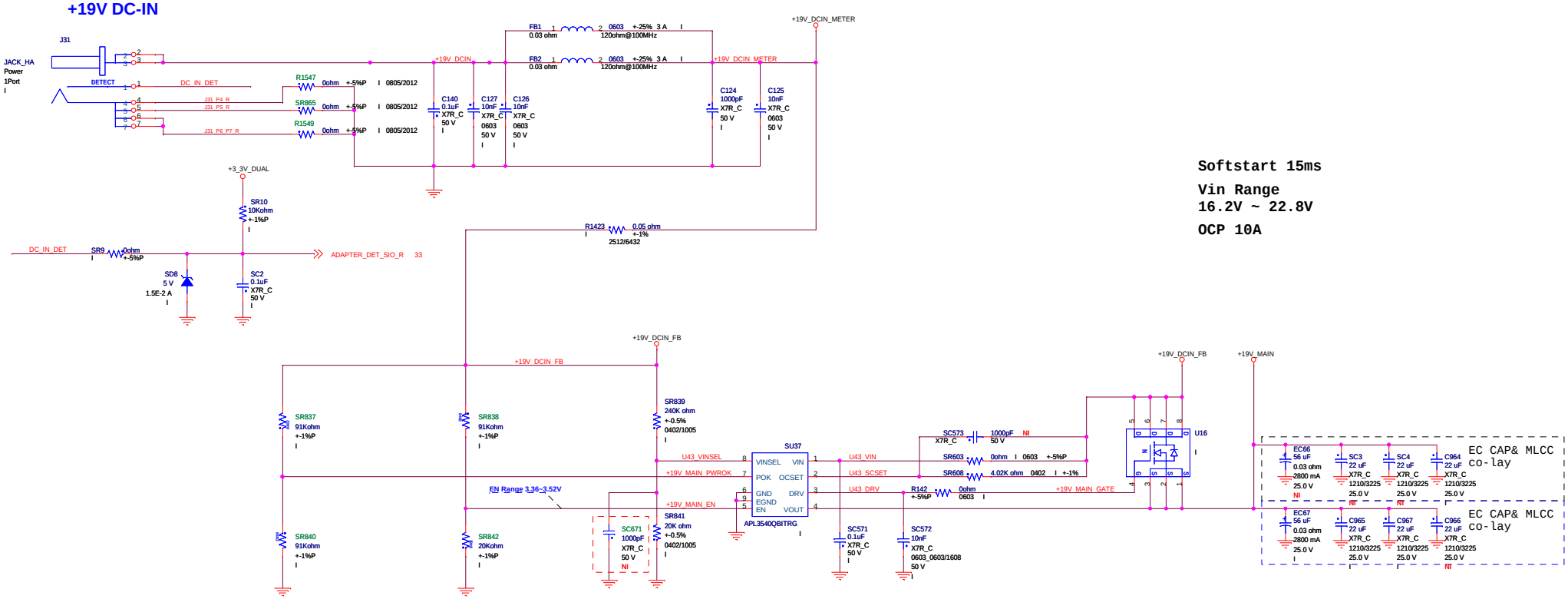
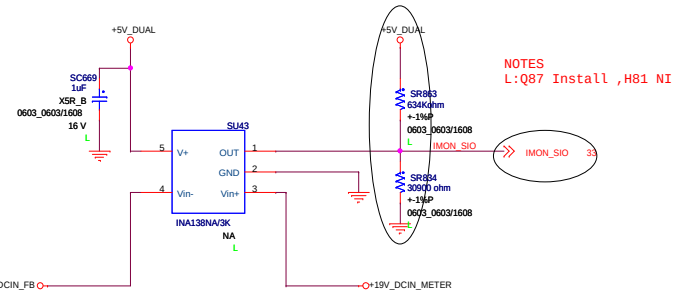
+19V DC-IN



Softstart 15ms

Vin Range
16.2V ~ 22.8V

OCP 10A



NOTES
L:Q87 Install ,H81 NI

LITE-ON TECHNOLOGY CORP.		LITEON
Title	49. DC +19V_MAIN / POWER METER	
Size C	Document Number JC184/JC186	Rev A01
Date: Wednesday, April 24, 2013	Sheet 49 of 62	

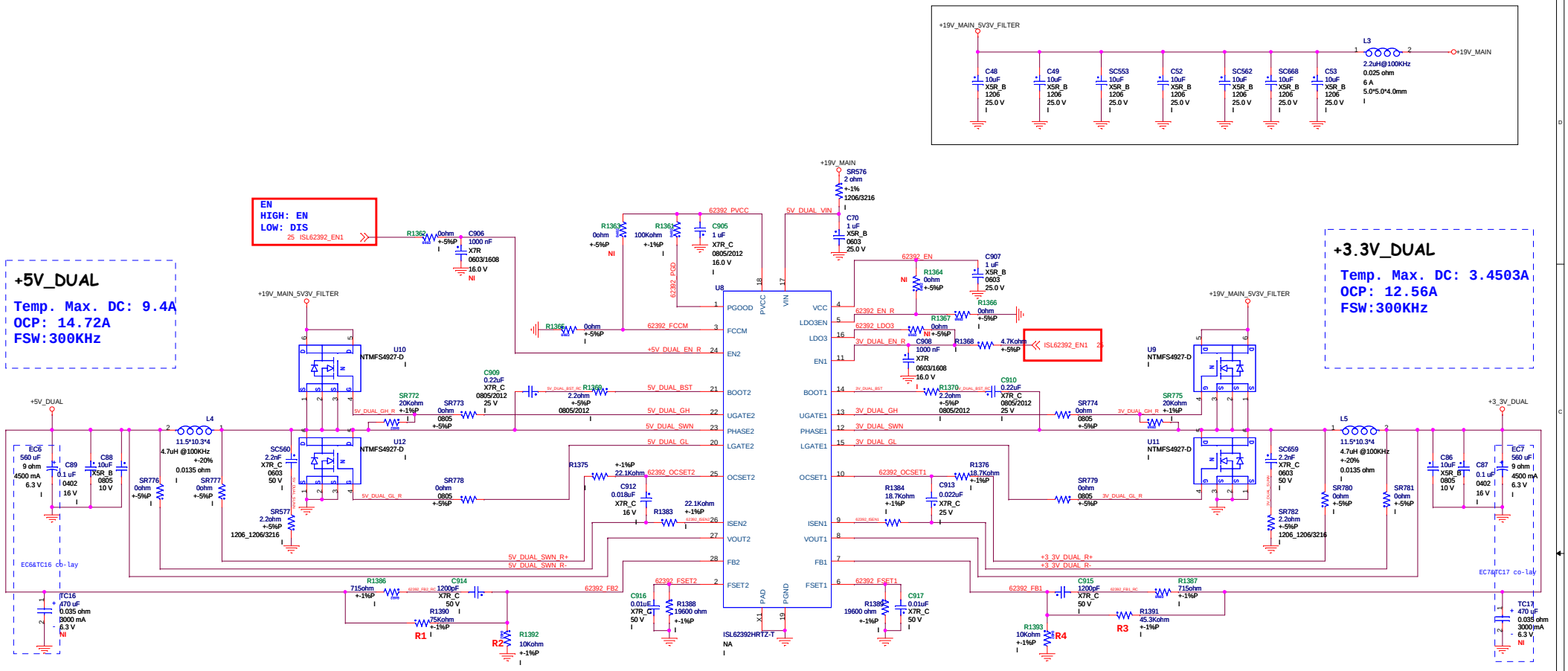


FIGURE 30. SYMMETRIC LAYOUT GUIDE

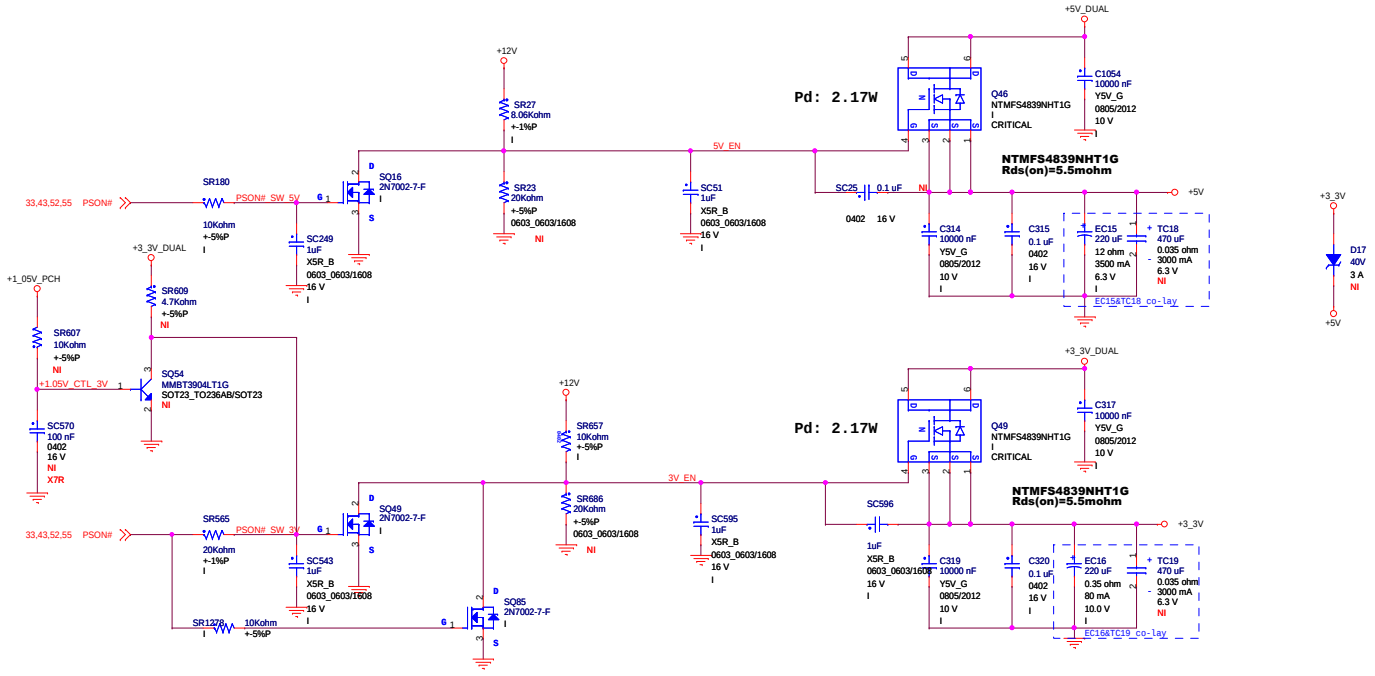
FCCM	Level(Efficiency Mode)
<0.8V	Low(DCM enabled)
1.9V~2.1V	Float (audio filter enabled)
>2.4v	Hign(forced CCM)

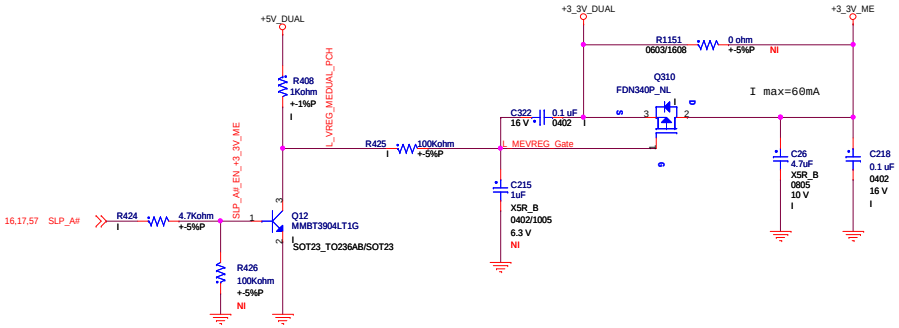
LITE-ON TECHNOLOGY CORP.

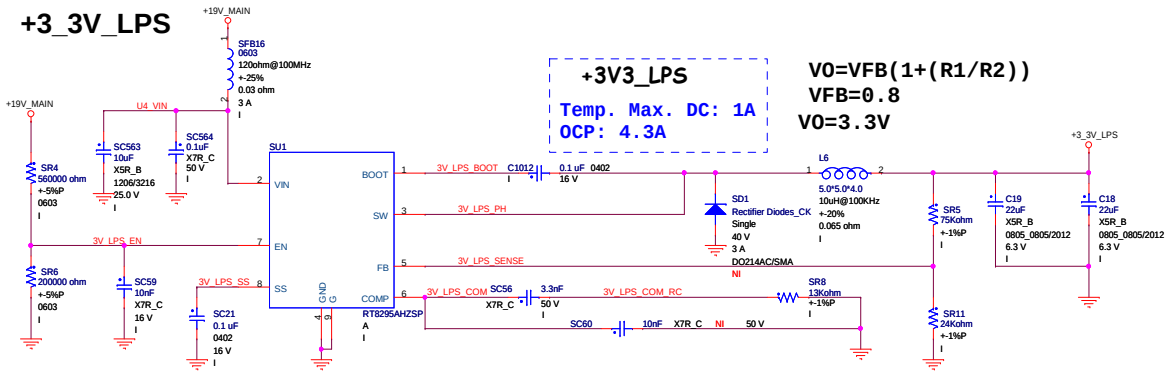
Title: 50. +5V_DUAL / +3_3V_DUAL

Size: Custom | Document Number: JC184/JC186 | Rev: A01

Date: Tuesday, April 23, 2013 | Sheet 50 of 62







LITE-ON TECHNOLOGY CORP.	LITEON	
Title	51. +5V/ +3.3V/ +3_3V_LPS/ ME	
Size C	Document Number JC184/JC186	Rev A01
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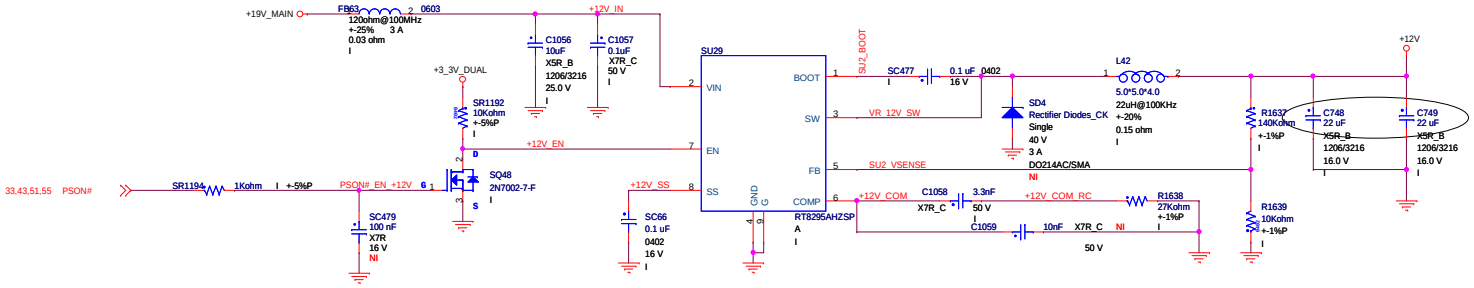
+12V

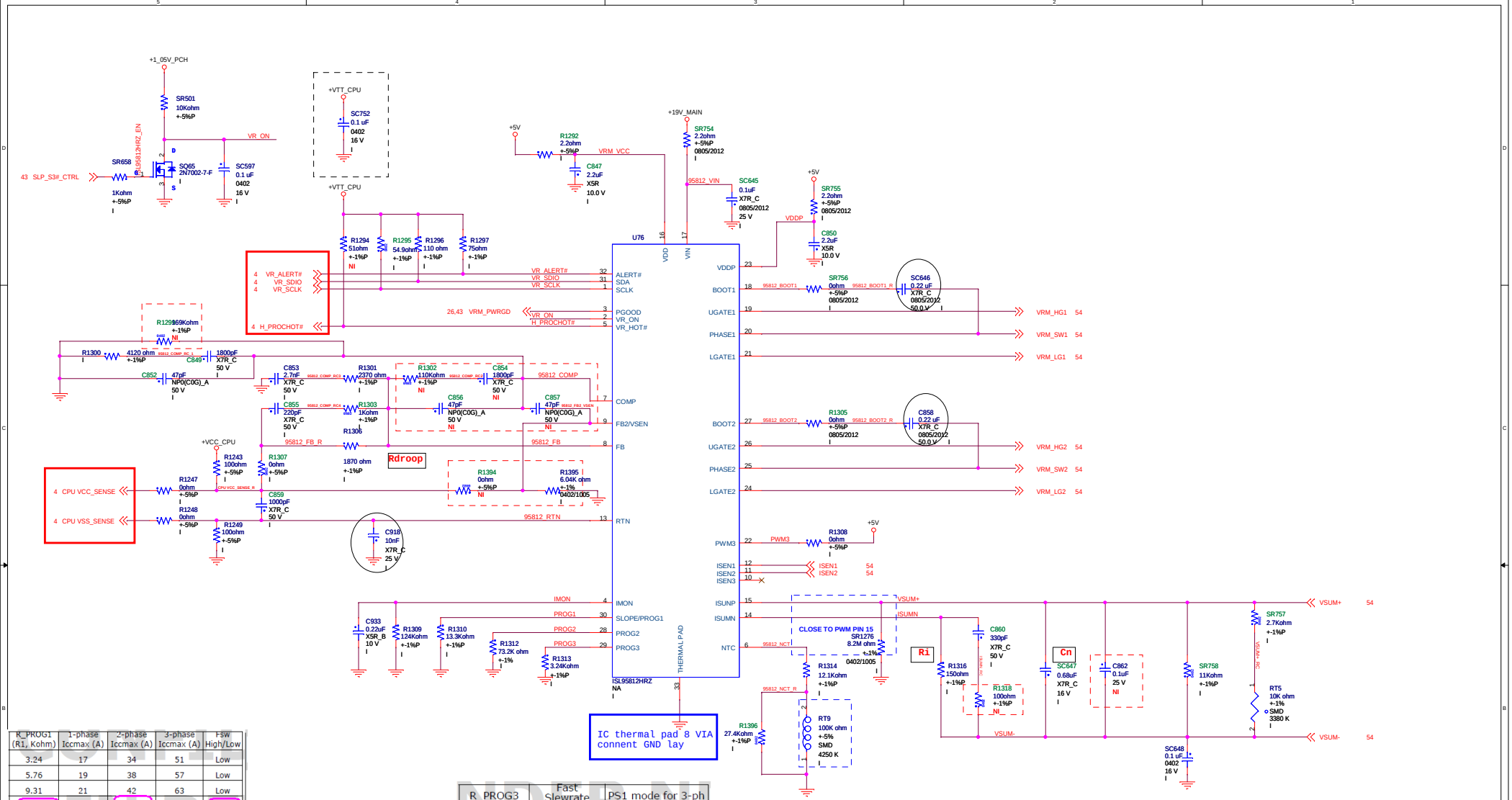


+12V

Temp. Max. DC: 0.7A
OCP: 4.3A

VO=VFB(1+(R1/R2))
VFB=0.8
VO=12.05V

LITE-ON TECHNOLOGY CORP.		LITEON
Title: 52. +12V		
Size: C	Document Number: JC184/JC186	Rev: A01
Date: Tuesday, April 23, 2013	Sheet 52 of 62	



R_PROG1 (R1, Kohm)	1-phase Iccmax (A)	2-phase Iccmax (A)	3-phase Iccmax (A)	Fsw High/Low
3.24	17	34	51	Low
5.76	19	38	57	Low
9.31	21	42	63	Low
13.3	24	48	72	Low
16.9	28	56	84	Low
21	33	66	99	Low
24.9	35	70	105	Low
28.7	38	76	114	Low
34	43	86	129	Low
42.2	48	96	144	Low
49.9	50	100	150	Low
57.6	55	110	165	Low
64.9	17	34	51	High
73.2	19	38	57	High
80.6	21	42	63	High
90.9	24	48	72	High
102	28	56	84	High
113	33	66	99	High
124	35	70	105	High
137	38	76	114	High
154	43	86	129	High
169	48	96	144	High
187	50	100	150	High
210	55	110	165	High

45W

R_PROG2 (R2, Kohm)	Fsw Low/High (KHz)	Vboot (V)
3.24	450/750	0
5.76	450/750	1.65
9.31	450/750	1.7
13.3	450/750	1.75
16.9	400/666	1.75
21	400/666	1.7
24.9	400/666	1.65
28.7	400/666	0
34	350/583	0
42.2	350/583	1.65
49.9	350/583	1.7
57.6	350/583	1.75
64.9	300/500	1.75
73.2	300/500	1.7
80.6	300/500	1.65
90.9	300/500	0

R_PROG3 (R3, Kohm)	Fast Slewrate (mV/uS)	PS1 mode for 3-ph Configruation
3.24	12	2-ph CCM
5.76	24	2-ph CCM
9.31	40	2-ph CCM
13.3	45	2-ph CCM
16.9	53	2-ph CCM
21	64	2-ph CCM
24.9	80	2-ph CCM
28.7	106	2-ph CCM
34	12	1-ph CCM
42.2	24	1-ph CCM
49.9	40	1-ph CCM
57.6	45	1-ph CCM
64.9	53	1-ph CCM
73.2	64	1-ph CCM
80.6	80	1-ph CCM
90.9	106	1-ph CCM

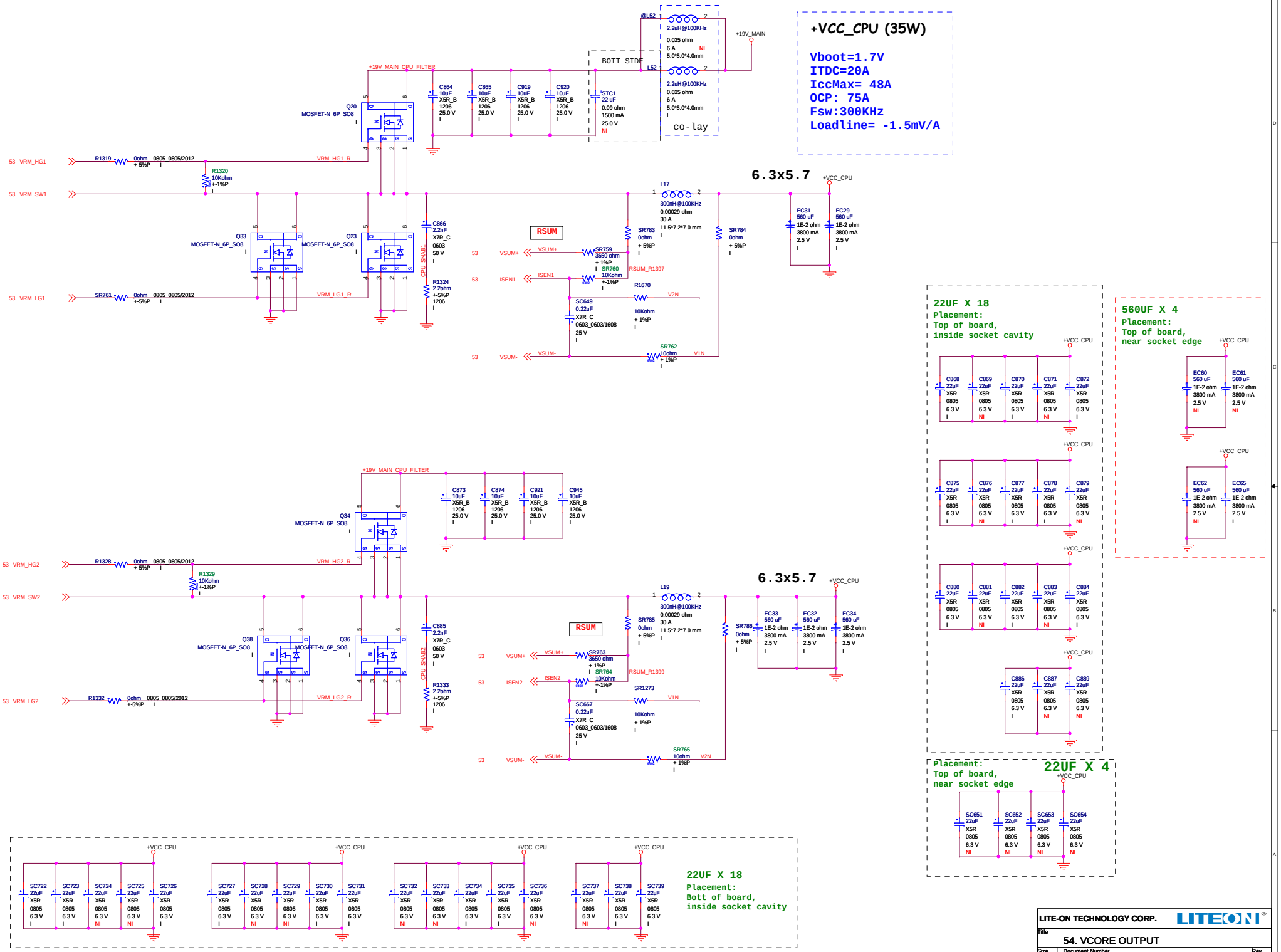
RELEASE

LITE-ON TECHNOLOGY CORP.

Title: 53. VCORE CONTROLLER

Size: C | Document Number: JC184/JC186 | Rev: A01

Date: Tuesday, April 23, 2013 | Sheet 53 of 62



LITE-ON TECHNOLOGY CORP.

Title: 54. VCORE OUTPUT

Size	Document Number	Rev
C	JC184/JC186	A01

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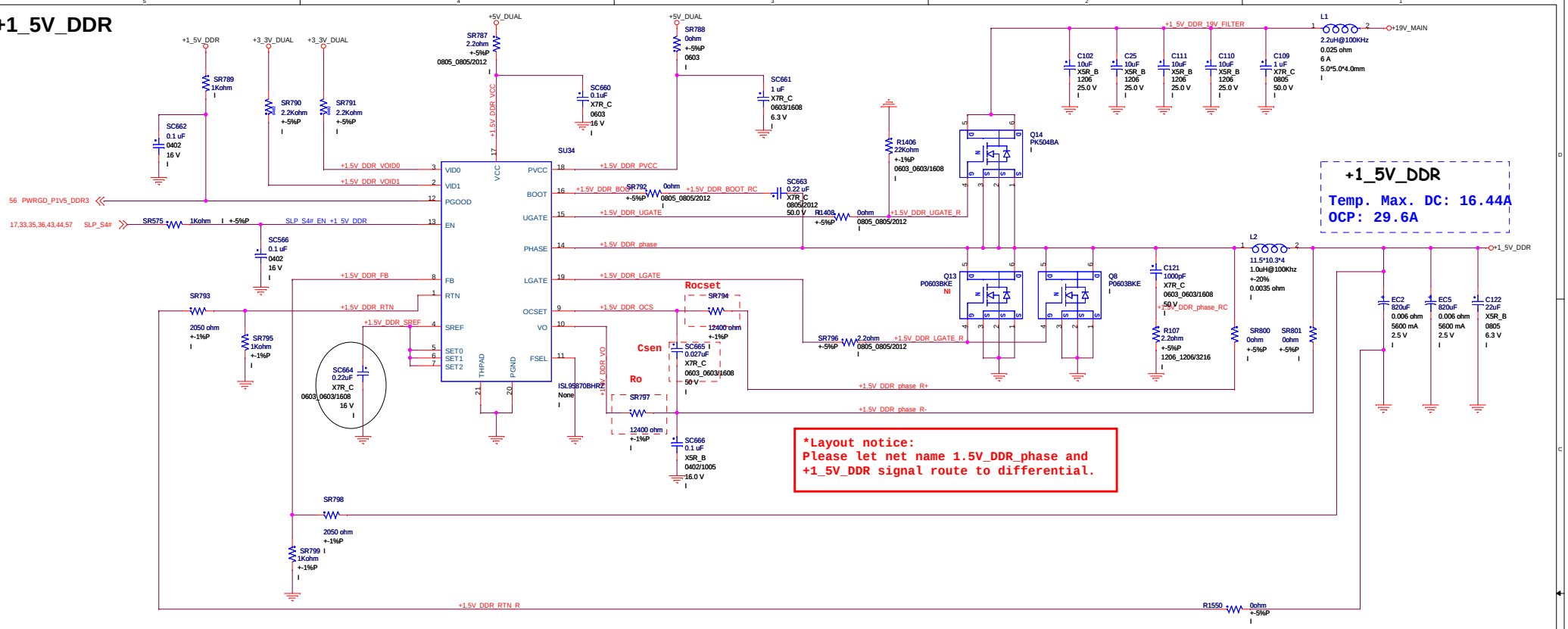
+1_5V_DDR



OCP

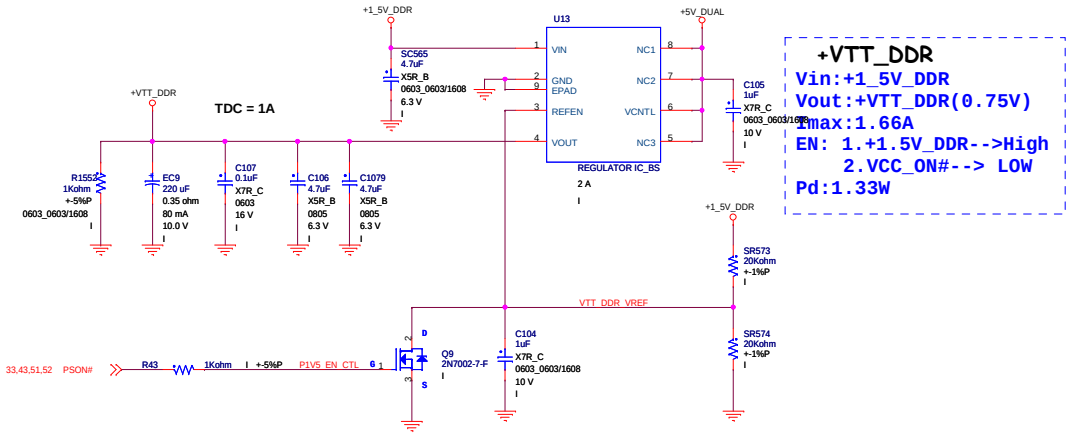
L=	1	uH
DCR=	3.5	m ohm
Ioc=	30	A
Csen=	27.21088	nF
Rocset=	10.5	K ohm
Ro=	10.5	K ohm

$$R_{OCSET} = \frac{I_{OC} \cdot DCR}{I_{OCSET}}$$

$$C_{SEN} = \frac{L}{R_{OCSET} \cdot DCR}$$

FSEL=>Pull this pin directly to GND for 300kHz.

check TINY SCH



LITE-ON TECHNOLOGY CORP.	LITEON
Title	55. +1.5V_DDR / +VTT_DDR
Size C	Document Number JC184/JC186
Rev	A01
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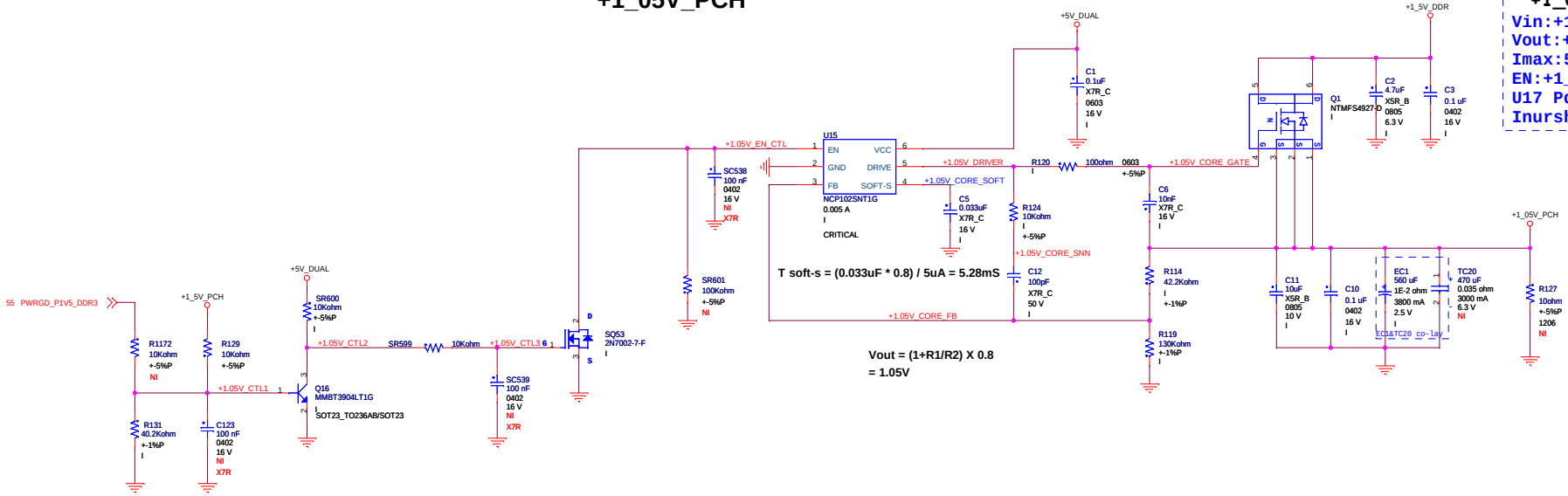
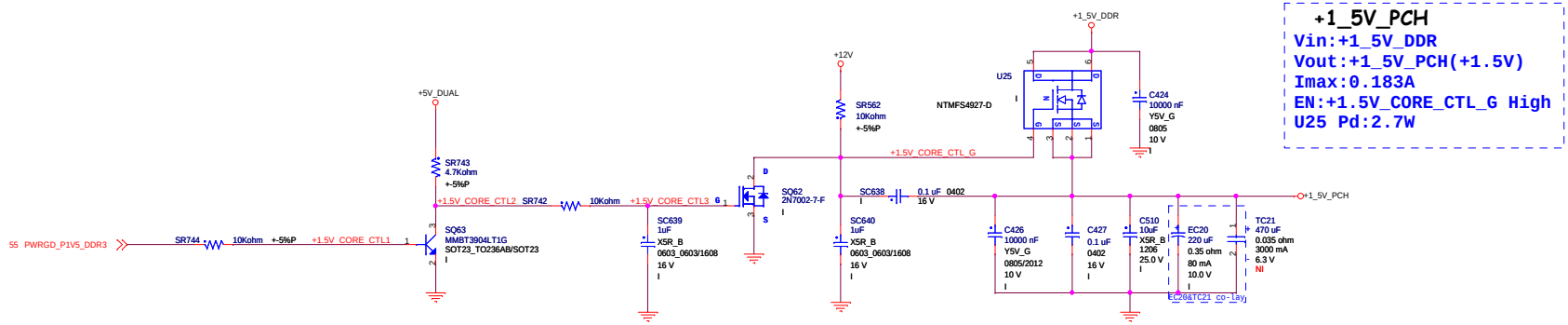
+1_05V_PCH

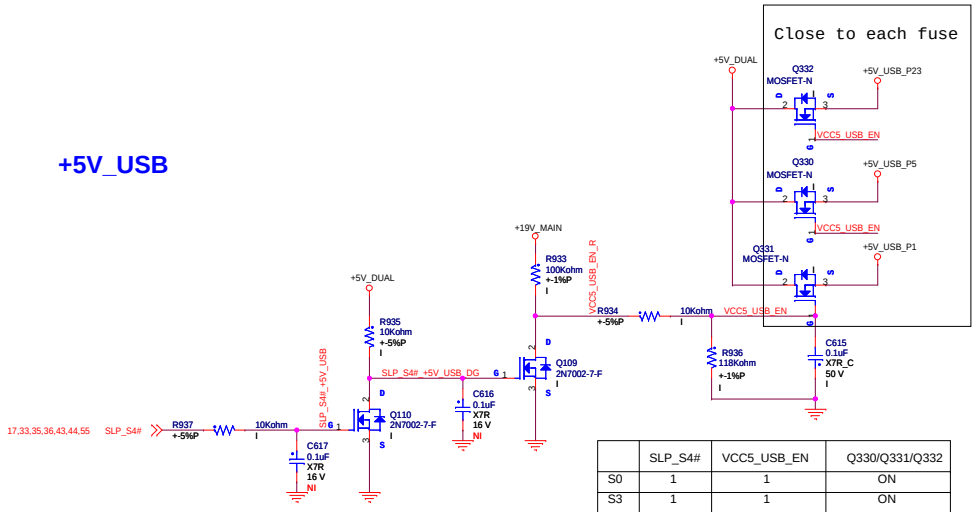


+1_5V_PCH

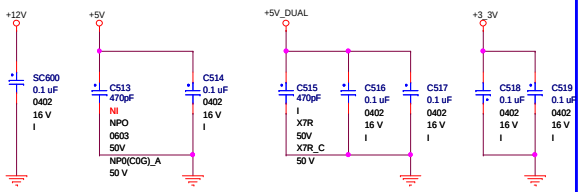


LITE-ON TECHNOLOGY CORP.		LITEON
Title	56. +1_5V_PCH /+1_05V_PCH	
Size C	Document Number JC184/JC186	Rev A01
Date: Tuesday, April 23, 2013	Sheet 56 of 62	

+5V_USB

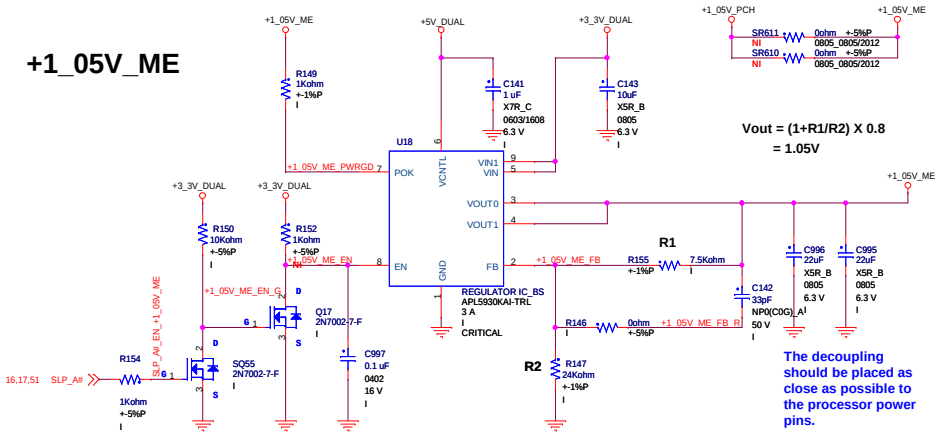


	SLP_S4#	VCC5_USB_EN	Q330/Q331/Q332
S0	1	1	ON
S3	1	1	ON
S4	0	0	OFF
S5	0	0	OFF



CAD NOTE: Place Around the Input Power Connectors

+1_05V_ME



Vout = (1+R1/R2) X 0.8
= 1.05V

The decoupling should be placed as close as possible to the processor power pins.

+1_05V_ME
Vin:+3_3V_DUAL
Vout:+1_05V_ME (+1.05V)
Imax:0.67A
Pd:2W

LITE-ON TECHNOLOGY CORP.		LITEON
Title: 57. +1_05V_ME / +5V_USB		
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PCH STRAPPING PIN

Signal	Usage	When Sampled	Comment
SPKR (S_SPKR_OUT)	No Reboot	Rising edge of PWROK	Set pull down. The signal has weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode
GPIO62 / SUSCLK (SUSCLK_GP62)	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	Set pull high. THis has a weak internal pull-up Note: The internal pull-up is disabled after RSMRST#
GPIO55	Top-Block Swap Override	Rising edge of PWROK	Set pull high. The signal has weak internal pull-up . If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
INTVRMEN (S_INTVRMEN)	Integrated V VRM Enable / Disable	Always	Set pull high. Integrated VRMs is enabled when INTVRMEN is sampled high
GPIO51	Boot BIOS Strap Bit[1] BBS[1]	Rising edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-up.
GPIO19 / SATA1GP	Boot BIOS Strap Bit[0] BBS[0]	Rising edge of PWROK	This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-up.
GPIO53	ESI Strap (Server/Workstation Only)	Rising edge of PWROK	Set pull high. This Signal has a weak internal pull-up.Tying this strap low configures DMI for ESI compatible operation.
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of PWROK	reserve pull up If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default) If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
GPIO36 (CLEAR_CMOS#)	RSVD	Rising edge of PWROK	Set pull high. This signal has a weak internal pull-down.
GPIO37 / SATA3GP (GPIO_37)	TLS Confidentiality	Rising edge of PWROK	Set pull high. This signal has a weak internal pull down. TLS CONFIDENTIALITY DISABLE LOW:DISABLE
DDPB_CTRLDATA (V_DDPB_CTRLCLK)	PORT B Detected	Rising edge of PWROK	When ‘1’- Port B is detected; When ‘0’- Port B is not detected. This signal has a weak internal pull-down.
DDPC_CTRLDATA (V_DDPC_CTRLDATA)	PORT C Detected	Rising edge of PWROK	When ‘1’- Port C is detected; When ‘0’- Port C is not detected. This signal has a weak internal pull-down.
DDPD_CTRLDATA (V_DDPD_CTRLDATA)	PORT D Detected	Rising edge of PWROK	When ‘1’- Port D is detected; When ‘0’- Port D is not detected. This signal has a weak internal pull-down.
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	Always	If strap is sampled high, the Integrated Deep Sx Well (DSW) On-Die VR mode is enabled.
GPIO36 / SATA2GP (CLEAR_CMOS#)	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTES: 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.
GPIO8 (IGE_EN#)	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-up. NOTES: 1. The internal pull-up is disabled after RSMRST# deasserts. 2. This signal should not be pulled low when strap is sampled.

PCH GPIO TABLE

GPIO	Signal Name	Power Well	In/Out	Tiny II
GPIO_0	BMBUSY-_GPIO0	VCC3	IN	SIO_SCI#
GPIO_1	TACH1_GPIO1	VCC3	IN	BRD_ID1
GPIO_2	PIRQE-_GPIO2	VCC3	IN	SIO_SCI1#
GPIO_3	PIRQF-_GPIO3	VCC3	IN	SIO_SCI2#
GPIO_4	PIRQG-_GPIO4	VCC3	NATIVE	GPIO_4(NO USE 8K2 PU)
GPIO_5	PIRQH-_GPIO5	VCC3	NATIVE	GPIO_5(NO USE 8K2 PU)
GPIO_6	TACH2_GPIO6	VCC3	IN	BRD_ID0
GPIO_7	TACH3_GPIO7	VCC3	IN	DP_C_DET#
GPIO_8	GPIO8	SB3V	IN	IGE_EN#
GPIO_9	OC5-_GPIO9	SB3V	NATIVE	OC5#_R_1011(NO USE 8K2 PU)
GPIO_10	OC6-_GPIO10	SB3V	OUT	OC6#_R_1213 (NO USE 8K2 PU)
GPIO_11	SMBALERT-_GPIO11	SB3V	IN	SIO_PME#
GPIO_12	LAN_PHY_PWR_CTRL_GPIO12	DSW	NATIVE	L_LAN_DISABLE#
GPIO_13	DA_DOCK_RST-_GPIO13	SB3V	OUT	PCH_GPIO13_PU(NO USE 10K PU)
GPIO_14	OC7-_GPIO14	SB3V	IN	OC7#_R_1415 (NO USE 8K2 PU)
GPIO_15	GPIO15	SB3V	IN	PCH_GP15_STRAP(NO USE 4.7K PU)
GPIO_16	SATA4GP_GPIO16	VCC3	NATIVE	MSATA_DET_GPIO16
GPIO_17	TACH0_GPIO17	VCC3	IN	BRD_ID3
GPIO_18	PCIECLKRQ1-_GPIO18	VCC3	IN	PCH_GP18 (NON USE 10K PD)
GPIO_19	SATA1GP_GPIO19	VCC3	IN	SATA1GP (10K PU/STRAP PIN)
GPIO_20	PCIECLKRQ2-_GPIO20_SMI-	VCC3	OUT	MINIPE_W_DISABLE#_2
GPIO_21	SATA0GP_GPIO21	VCC3	IN	THRM_ID1
GPIO_22	SCLOCK_GPIO22	VCC3	IN	GPIO_22 (NON USE 10K PU)
GPIO_23	LDRQ1-_GPIO23	VCC3	NATIVE	GPIO_23(NON USE)
GPIO_24	GPIO24	SB3V	IN	H_SKTOCC#
GPIO_25	PCIECLKRQ3-_GPIO25	SB3V	OUT	MINIPE_W_DISABLE#_1
GPIO_26	PCIECLKRQ4-_GPIO26	SB3V	IN	GP26_PD (NON USE 10K PD)
GPIO_27	GPIO27	DSW	IN	LANWAKE_R_N
GPIO_28	GPIO28	SB3V	OUT	PW_LED#
GPIO_29	SLP_WLAN-_GPIO29	DSW	NATIVE	PCH_GPIO29_PU(NON USE 10K PU)
GPIO_30	SUSWARN-_SUSPWRNACK_GPIO30	SB3V	NATIVE	SUSWARN#
GPIO_31	ACPRESENT_GPIO31	DSW	OUT	SUS_LED#
GPIO_32	GPIO32	VCC3	OUT	TPM_CLKRUN (NON USE)
GPIO_33	DOCKEN-_GPIO33	VCC3	IN	PCH_GP33 (NON USE 10K PD)
GPIO_34	GPIO34	VCC3	IN	BRD_ID2
GPIO_35	GPIO35_NMI-	VCC3	IN	USB_DET#
GPIO_36	SATA2GP_GPIO36	VCC3	IN	CLEAR_CMOS#(STRAP PIN)
GPIO_37	SATA3GP_GPIO37	VCC3	IN	GPIO_37 (STRAP PIN)
GPIO_38	SLOAD_GPIO38	VCC3	IN	GPIO_38(NON USE 10K PU)
GPIO_39	SDATAOUT0_GPIO39	VCC3	IN	GP39_GFX_CRB_DETECT
GPIO_40	OC1-_GPIO40	SB3V	NATIVE	USB_OC_REAR_23#
GPIO_41	OC2-_GPIO41	SB3V	NATIVE	USB_OC_REAR_45#
GPIO_42	OC3-_GPIO42	SB3V	OUT	MINIPE_W_DISABLE#
GPIO_43	OC4-_GPIO43	SB3V	NATIVE	USB_OC_REAR_89# (NON USE 8.2K PU)
GPIO_44	PCIECLKRQ5-_GPIO44	SB3V	OUT	BAT_LED#
GPIO_45	PCIECLKRQ6-_GPIO45	SB3V	IN	PRT_DET#
GPIO_46	PCIECLKRQ7-_GPIO46	SB3V	OUT	TPM_DISABLE#
GPIO_48	SDATAOUT1_GPIO48	VCC3	IN	COM_AB_DET#
GPIO_49	SATA5GP_GPIO49	VCC3	IN	NON USE 10K PU
GPIO_50	GPIO50	VCC3	OUT	GPIO_50
GPIO_51	GPIO51	VCC3	NATIVE	GPIO_51 (STRAP PIN)
GPIO_52	GPIO52	VCC3	IN	COM_A_DET#
GPIO_53	GPIO53	VCC3	IN	NON USE (STRAP PIN)
GPIO_54	GPIO54	VCC3	IN	GPIO_54 (NON USE 8.2K PU)
GPIO_55	GPIO55	VCC3	NATIVE	NON USE (STRAP PIN)
GPIO_57	GPIO57	SB3V	IN	NON USE 10K PU
GPIO_58	SML1CLK_GPIO58	SB3V	NATIVE	SMLINK1_CLK
GPIO_59	OC0-_GPIO59	SB3V	NATIVE	USB_OC_FRONT_01#
GPIO_60	SML0ALERT-_GPIO60	SB3V	IN	SMB0_ALERT#
GPIO_61	SUS_STAT-_GPIO61	SB3V	NATIVE	TPM_LPC_PD#
GPIO_62	SUSCLK_GPIO62	SB3V	NATIVE	SUSCLK_GP62 (STRAP PIN)
GPIO_63	SLP_S5-_GPIO63	SB3V	NATIVE	TP (NO USE)
GPIO_64	CLKOUTFLEX0_GPIO64	VCC3	NATIVE	TP (NO USE)
GPIO_65	CLKOUTFLEX1_GPIO65	VCC3	NATIVE	LPC_ MINI_MSATA
GPIO_66	CLKOUTFLEX2_GPIO66	VCC3	NATIVE	TP (NO USE)
GPIO_67	CLKOUTFLEX3_GPIO67	VCC3	NATIVE(ITE) GPO(nuvoton)	CK_48M_SIO
GPIO_68	TACH4_GPIO68	VCC3	IN	LC_SENSE
GPIO_69	TACH5_GPIO69	VCC3	IN	THRM_ID2
GPIO_70	TACH6_GPIO70	VCC3	IN	PCH_GP70_PU
GPIO_71	TACH7_GPIO71	VCC3	IN	BRD_ID5
GPIO_72	GPIO72	DSW	OUT	PCH_GP72_PU (NON USE 1K PU)
GPIO_73	PCIECLKRQ0-_GPIO73	SB3V	IN	GP73_PD(NON USE 10K PD)
GPIO_74	SML1ALERT-_PCHHOT-_GPIO74	SB3V	NATIVE	PCH_GP74_PU(NON USE 10K PU)
GPIO_75	SML1DATA_GPIO75	SB3V	NATIVE	SMLINK1_DATA

SIO IT8733F GPIO TABLE		
GPIO	Signal Name	**Tiny II**
GPIO_10(PIN84)	PCIRST3#/GP10	DP_ESIO (PU SB3V)
GPIO_11(PIN34)	PCIRST2#/GP11	+19V_VIN CTL_SIO (PU SB3V)
GPIO_12(PIN33)	PCIRST1#/GP12	(NO USE)
GPIO_13(PIN32)	PWROK1/GP13	SIO_PWRGD_3V
GPIO_14(PIN31)	VCORE_EN/PCH_C1/GP14	SMLINK1_CLK
GPIO_15(PIN3)	PCIRSTIN#/CIRTX2/GP15/CPU_PG	SIO_SCI2# (PU +3.3V)
GPIO_16(PIN2)	5VSB_CTRL#/CIRRX2/GP16	SIO_SCI1# (PU +3.3V)
GPIO_17(PIN28)	RI2#/GP17	RI2-
GPIO_20(PIN27)	CTS2#/GP20	CTS2-
GPIO_21(PIN26)	DCD2#/GP21	DCD2-
GPIO_22(PIN25)	SCK/GP22	SIO_SCK
GPIO_23(PIN24)	SI/GP23	SIO_SI
GPIO_24(PIN23)	RTS2#/GP24	RTS2-
GPIO_25(PIN22)	DSR2#/GP25	DSR2-
GPIO_26(PIN21)	SOUT2/GP26	SOUT2-
GPIO_27(PIN20)	SIN2/GP27	SIN2-
GPIO_30(PIN19)	ATXPG/GP30	PWRGD_PS
GPIO_31(PIN18)	PWMOUT / GP31 / USBPWREN2#	SIO_CHR_USBPWREN (PU SB3V)
GPIO_32(PIN17)	DPWROK/GP32	SIO_GP32(NO USE)
GPIO_33(PIN16)	SUSACK#/GP33	SIO_PIN16_EC(4.7K PD)
GPIO_34(PIN15)	SUSWARN#/GP34	(NO USE)
GPIO_35(PIN14)	FAN_TAC4/GP35	INT1_G_SIO
GPIO_36(PIN13)	FAN_CTL3/GP36	INT2_G_SIO
GPIO_37(PIN12)	FAN_TAC3/GP37	SIO_PIN12(NO USE 4.7K PU)
GPIO_40(PIN79)	3VSBSW#/GP40	ME_CNTL
GPIO_41(PIN78)	PWROK2/GP41	SIO_SCI#
GPIO_42(PIN76)	PSON#/GP42	SIO_PSON#
GPIO_43(PIN75)	PANSWH#/GP43	SIO_PB_IN
GPIO_44(PIN72)	PWRON#/GP44	PWRBTN_OUT#
GPIO_46(PIN66)	D_RX0/SMBCLK2/GP46/IRRX	SIO_RTCX2
GPIO_47(PIN65)	D_TX0/SMDAT2/GP47	SIO_RTCX1
GPIO_50(PIN48)	SO/GP50	SIO_SO
GPIO_51(PIN11)	FAN_CTL2/GP51	(NO USE)
GPIO_52(PIN10)	FAN_TAC2/GP52	SIO_PIN10(NO USE 4.7K PU)
GPIO_53(PIN77)	SUSC#/GP53	SLP_S4#
GPIO_54(PIN73)	PME#/GP54/USBPWREN1#	SIO_PME#
GPIO_55(PIN85)	RSMRST#/CIRRX1/GP55	RSMRST_N_SIO
GPIO_56(PIN83)	MCLK/GP56	2543_CLT1 (PU SB3V)
GPIO_57(PIN82)	MDAT/GP57	2543_EN (PU SB3V)
GPIO_60(PIN81)	KCLK/GP60	2543_CLT3 (PU SB3V)
GPIO_61(PIN80)	KDAT/GP61	CHARGER_OC_SIO# (PU SB3V)
GPIO_62(PIN45)	KRST#/GP62	KBRST#
GPIO_63(PIN6)	SLP_SUS#/VLDT_EN/GP63	5V_DUAL_DISABLE#
GPIO_70(PIN113)	KSI0/GP70/PD0	PD0
GPIO_71(PIN114)	KSI1/GP71/PD1	PD1
GPIO_72(PIN115)	JP1/KSO0/GP72/PD2	PD2
GPIO_73(PIN116)	KSO1/GP73/PD3	PD3
GPIO_74(PIN117)	KSO2/GP74/PD4	PD4
GPIO_75(PIN118)	KSO3/GP75/PD5	PD5
GPIO_76(PIN119)	KSO4/GP76/PD6	PD6
GPIO_77(PIN120)	KSO5/GP77/PD7	PD7
GPIO_85(PIN64)	IO_SCI#/GP85/SMBDAT0	APS_I2C_DATA
GPIO_86(PIN63)	GP86/SMBCLK0	APS_I2C_CLK

X02 to X04 09292012

(1) Page 29, Add DP port C redriver IC and schematic.

(2) Page 40, Connect J33 pin 19,20,21,23 to GND

(3) Page 20, Switch LPC_ MINI_MSATA from 33M port 3 to port 0
Switch C_PCI_SB from 33M port 0 to port 2
Switch CK_33M_SIO from 33M port 2 to port 3
Switch C_PCIE_LAN1(+/-) from SRCCLK port 5 to port 2
Switch C_PCIEX1_1(+/-) from SRCCLK port 4 to port 1

(4) Page 15, Switch GLAN_RXP/N from PCIe port 6 to port 3
Switch GLAN_TXP/N from PCIe port 6 to port 3

(5) Page 33, Add Y2, C58, C61, R190 for SIO Xtal 32.768K

(6) Page 33, Switch INT1_G_SIO from SU41 pin 63 to pin 14
Switch INT2_G_SIO from SU41 pin 64 to pin 13
Switch APS_I2C_DATA from SU41 pin 65 to pin 64
Switch APS_I2C_CLK from SU41 pin 66 to pin 63
Connect SIO_RTCX1 to SU41 pin 65
Connect SIO_RTCX2 to SU41 pin 66

X04 10012012A

(1) Page 20, Remove R1598,R1599 for WiFi layout routing.

(2) Page 14, Remove TP302,TP303,TP304,TP305 for layout routing.
Page 15, Remove TP306,TP307,TP308,TP309 for layout routing.
Page 23, Remove TP348 for layout routing.

X04 10012012B

(1) Page 20, Remove R1662,R1663,R1656,R1657 for DP(ck505 reserved)

(2) Page 4, add C1069 for PLTRST_CPU# signal have no-monotonic after power up

(3) Page 51, change SR565 to 24.9k to delay +3.3V

(4) Page 33, add C1072 for PCH_PLT_RST# signal(SU35 side) have no-monotonic after power up.

(5) Page 38, add C1073 for PCH_PLT_RST# signal(MSATA side) have no-monotonic after power up.

(6) Page 17, add SC715 for PWRGD_DRAM signal have no-monotonic after power down.

(7) Page 33, change SR703 to 1k for VCCST_PWRGD and PCH_PWROK signal Voltage less than 3.3v.
change SR719 I to NI for PCH_DPWROK signal have a step after power up.
(8) Page 31, add C1071 for PCH_PLT_RST# signal(Lan side) have no-monotonic after power up.

(9) Page 43, Rework R1592 pull high from 3.3V_DUAL to +3.3V for S_PCH_SYSPWROK
signal have a step after power up.
(10) Page 4, change SR333,SR336,SR340 to NI for H_PROCHOT# signal have a step after power up
and power down.
(11) Page 4, add C1070 for PWRGD_CPU signal have no-monotonic after power up and power down.

(12) Page 33, remove TP43 and Add SR1271 pull high toSIO_SB3V for ME disable,
P17 add R1665,R1666,Q436 for ME_CNTL SCH

X04 10032012

(1) Page 20, Switch LPC_ MINI_MSATA from 33M port 0(U2G-AV5) to GPIO65 (U2G-AT9)

(2) Page 15, Switch PCIE_RXP5/N5 from PCIe port 5 to port 4
Switch PCIE_TXP5_R/N5_R from PCIe port 5 to port 4

(3) Page 36, change EC64 from 560uf DIP to SMT component for ME concern

(4) Page 17, change R1648 to NI and switch pull high from +3V3 to 3V3_DUAL

(5) Page 50, change C908 from NI to 1uF, and R1368 from 0 ohm to 4.7K ohm
Page 31, change SR636 from 220 ohm to 2K ohm for LAN 3.3V pwr on sequency

(6) Page 55, change SR793 SR795 from 2K to 2.05K 1%(DDR_VTT)

(7) Page 43, modify PCH_VRMPWRGD circuit

(8) Page 36, modify USB Charger CTL1, CTL2, CTL3, EN, ILIM
Page 33, modify SIO connect to Charger IC pin CTL1, CTL2, CTL3, EN
(9) Page 36, remove U84(ESD) for layout routing.
Change SU42 from Semtech to Amazing vendor
(10) Page 42, Change VGA ESD from 7 pcs Semtech to 2 pcs Amazing vendor, footprint from 0402 to SOT23-6

X04 10052012

(1) Page 53, Vcore controller circuit,Change R1300,R1301,C853,R1306,R1310,R1316,R1313,R1309
and install R1395 to 6.04k
(2) Page 54, Vcore output ,EC60,EC61,EC62 to NI

(3) Page 55, +1_5V_DDR, Change SR796,SR794,SR797,SR798

(4) Page 36, USB Charger,R1343 change to 47.5k ohm

(5) Page 30, Audio, Change D46,D47,D48,D49,D50,D51(pop noise)

(6) Page 34, Internal USB Change ESD U21

(7) Page 36, USB Charger Change ESD SU42

(8) Page 42, VGA ESD Change ESD U32,U33

(9) Page 30, AUDIO, R137 Change to 10ohm ,Remove SC658,add R1677 to 820 ohm for HD BUS (A_Z_SDOUT & A_Z_SDIN2)

X04 10062012

(1) Page 15&Page 17, NET NAME FROM PCIE_RXN5/ PCIE_RXP5 CHANGE TO PCIE_RXN4/PCIE_RXP4
FROM PCIE_TXN5_R/ PCIE_TXP5_R CHANGE TO PCIE_TXN4_R/ PCIE_TXP4_R
(2) Page 17, Switch MINIPE_W_DISABLE#_2 FROM GPIO57 TO GPIO20.
Switch PCH_GPIO20_PU FROM GPIO20 TO GPIO57(PCH_GPIO57_PU).
ADD GPIO25 R1652 10k PU (MINIPE_W_DISABLE#_1) for MSATA USE.

X04 10082013

(1) Page 33, SR708 NI to I , SR728 change to 100K for SIO

(2) Page 33, add SR1274 4.7k PD for SIO FW DET

(3) Page 54, add SC722,SC723,SC724,SC725,SC726,SC727,SC728,SC729,SC730,SC731,SC732,SC733,SC734,SC735,SC736,SC737,SC738,SC739
to NI for VCC_CPU,Remove SC678,SC679,SC683,SC684,SC685,SC686,SC687,SC688,SC689,SC690 for VCC_CPU
(4) Page 8, add SC740,SC741,SC742,SC743,SC744,SC745,SC746,SC747,SC748,SC749,SC750 to NI for 1_5V_DDR,

(5) Page 55, add C1079 for VTT_DDR

(6) Page 50, change U9,U10,U11,U12 MOSFET for 5V_DUAL ,3_3V_DUAL

X04 10092012

(1) Page 4, Move SC10 to CPU side for PWRGD_DRAM.

(2) Page 17, change C56 to 12pF,C57 to 15pF for 32.768KHz XTAL

(3) Page 29, SR30 to NI for redriver IC, add DP port C switch schematic.

X04 10112012

(1) Page 26, SXDP1 schematic change to NI

(2) Page 30, change SC655,SC656 to 100pF for MONO_OUT

X04 10122012

(1) Page 4, R1264 to NI for thermal test (VR_ALERT#_R)

X04 10162012

(1) Page 30, change SR1245 to NI,SR1246 to I for MONO_OUT

(2) Page 49, change SR863 to 619k ohm,SR834 change to 34.8k ohm for Power meter SCH.

(3) Page 32, Change SU9 from Nuvoton to ST vendor
SR64,SC676,SC33,SR55-->NI
R1583,C975,C1008,SR54-->I

X04 10172012

(1) Page 53, R1294 to NI for H_PROCHOT#

X04 to X05 10192012

(1) Page 53, R1306 change to 1.47k,R1309 change to
102k,R1316 change to 130 ohm, add SR1276 4.7M PD for IMON
(2) Page 37, J7 37PIN add SR1275 0ohm(NI) PD for WiFi card

X05 11022012

(1) Page 33, remove SR843,SR846,SR732,SR735,SR736,SR737 for SIO (USB Port4)
Add R1671 33ohm for EC SPI damping.
Change SU41 symbol Ver: BX to CX

X05 11072012

(1) Page 33& P49 , add Adapter_DET SCH (SR9,SR10,SD8,SC2,R10,R11),Change SR708 to NI for Adapder_DET(SIO pin95)

(2) Page 30, change SR1245 to I, SR1246 to NI for MONO_OUT

(3) Page 29, change SR69 to NI for DP redriver

(4) Page 47, del LTCT1, add ISN, add LTCT2 to NI,add @J8 for table.

(5) Page 35& 43, change U85,U86,U87 Vender to DII

X05 11082012

(1) Page 31 , change L7 footprint

X05 11092012

(1) Page 34 , move D60 close to P7, change D59 symbol for ESD

(2) Page 40 ,del SR668,SR671,SR667,SR683,SR670,SR680,SR681,SR682, add SC100~SC116 470 pF for Print port SCH

(3) Page 54 , add STC1,STC2,STC3 to NI for VCORE

(4) Page 33 , add SC751 0.1uF for SIO

(5) Page 36 , change D24 symbol for ESD

(6) Page 34 , change D60 symbol, C1055 to I for ESD

X05 11122012

(1) Page 34&36 , add C1097,C1098,C1099,C1100 0.1uF for EMI/EMC.

(2) Page 53 , change net PSON# to SLP_S3#_CTRL for Sequence(VR_EN to VR_Ready timing fai)

(3) Page 43 , SC718 change to 0.22uF, R1599 change to 330K ohm, C1074 change to 0.47uF, SC49 change to I for Sequence
(SYS_PWROK have a pulse before power up at G3 to S0 mode)
(4) Page 51 ,Change SR565 to 20K ohm for Sequence(Vboot ramp to VR_READY timing fail at S0 to S5 mode, G3 to S5),
SR27 change to 8.06 Kohm for Sequence (3.3v than 5v fast after power up at G3 to S5 mode)

X05 11132012

(1) Page 30 , add workaround SCH for AUDIO.

(2) Page 18 , Change SC633 from 1uf to 10uF for DC power(The V_1P5_DAC_FB_R signal have glitch when
change screen under windows OS. Test results very margin)
(3) Page 35 , change D5,D56,D57 symbol for ESD

(4) Page 33&49 , SR730,SR731,SR839,SR841 Tolerance from 1% change to 0.5%

(5) Page 8&54 , chenge SC723,SC727,SC731,SC735,SC739,SC722,SC726,SC730,SC734,SC738,SC740,SC742,SC744,SC746,SC748,SC750,SC749to I,C869,
C887,C881,C876,C883,C879,C871,C889,C1003,C998,C1005,C1006 to NI for CPU noise

X05 11202012

(1) Page 35 , R962 from PU +5V_DUAL change to +3_3V_DUAL for SIO POWER WELL

(2) Page 33 , SC716,SC717 change vender to WALSIN

(3) Page 54 , add @L52 co-lay for Vcore output (+19V_MAIN IN)

X06 11282012

(1) Page 42 , add D62 for VGA BLUE signal for TVS,modify U33 pin1 & pin3 (BLUE parallel) need change layout for TVS.

(2) Page 16 , SR585 change to I for KBRST#

X06 11292012

(1) Page 31 , change J8(RJ45) to non surge connect

(2) Page 53 , change R1316 to 150ohm, R1306 to 1.6K ohm,R1309 to 1.07Kohm, SR1276 to 8.2M for VCORE

(3) Page 50 , change R1375,R1383 to 22.1K ohm, R1376,R1384 to 18.7K ohm, C192 to 0.018uF,C193 to 0.022uF for +5V_DUAL / +3_3V_DUAL

X06 11302012

(1) Page 30 , modify audio Sleeve / Ring2 SCH

X06 12032012

(1) Page 53 , change R1306 to 1.87K ohm for VCORE CONTROLLER,add SC752 for +VTT_CPU Power

(2) Page 49 , del SC3,SC4,C964,C965,C966,C967, add EC66,EC67 for +19V_MAIN

(3) Page 54 , dChange SC651,SC652,SC653,SC654 to NI,del STC2,STC3 for VCORE OUTPUT

X06 12042012
(1) Page 43&P51 , add SR1277,SR1278,SQ85 for VccCore have No-Monotonic after power down at S0 to S5 mode
(2) Page 33 , add SC753 for IMON_SIO
(3) Page 49 , add (co-lay) C962,C963,C964,C965,C966,C967, change EC66,EC67 to DIP type for +19V_MAIN
(4) Page 17 , modify ME_disable sch (add R1678)

X06 12052012
(1) Page 50/54/55 , change C864,C865,C919,C920,C873,C874,C921,C945,C102,C25,C110,C111 C48,C49,SC553,C52,SC562,SC668,C53 vendor for CPU noise
(2) Page 29 , add R1679 0ohm to NI for redriver sch

X06 12062012
(1) Page 55 , change SR795 to 1K ohm for +1_5V_DDR
(2) Page 26 , change SR626,SR629 to I,@J21(1-3)1,@J20(1-3)1, J21,J20 to NI for SPI ROM SCH.
(3) Page 29 , change SC593,SC594,SC626,SC701,SC702,SC703,SC704,SC705,SC706,SC707,SC708, SC709,SC710,SC712,SC713,SC714,SR19,SR20,SR21,SR22,SR30,SR34,SR35,SR36,SR67,SR68,SR70, SU2,C962,C963,Q118,R20,R21 to C30,C31,C32,C33,C34,C35,C36,C37,C38,C61,C62,C63,C64,C65, C66,C67,R45,R46,R47,R48,R49,R50,R51,R52,R53,R54,R55,U1,SC3,SC4,SQ1,SR1,SR2 (Redriver IC from bottom side move to top side)
(4) Page 26&P31 , change C56 to 15pF for Y1 32.768k crystal (PCH), SC462 to 27pF for SY1 25MHz crystal (LAN)

X06 12072012
(1) Page 30 , change R1677 to I, R1676 to NI for audio noise(G3 mode)

X07 12172012
(1) Page 18 , change netname, from PCH_GP71_PU change to BRD_ID5
(2) Page 40 , change SQ77 vendor, from DII change to PANJIT

X07 12242012
(1) Page 49 , SC573 change to NI,SC572 change to 10nF for 19V_MAIN OCP issue with Battery BOX.
(2) Page 53 , R1314 change to 7.5Kohm for L17 thermal protection point.
(3) Page 30&47 , add R1680 0ohm for Digital GNDand analog GND,add R1681 0ohm for FAN DUCT to GND.

X07 12262012
(1) Page 32 , SU9 change symbol to ST33ZP24AR28PVSP (TPM)
(2) Page 55 , Q8,Q14 change Vender to NIKO

X07 01022013
(1) Page 31 , change Foxconn RJ45 connect to JFM3811B-2104-4F (Return Loss)
(2) Page 36 , change USB charger IC to TP2546
(3) Page 30/42/45 , change Q28,Q29,Q31,SQ59,SQ60 to 2N7002KW
(4) Page 24 , change @E1(1-2) to H=6mm
(5) Page 25 , add PCH_RSMRST# Pull down SCH.

X07 01082013
(1) Page 14~21,23 change PCH U2 sysmbol to DH82Q87 QE8X
(2) Page 31 , change SU10 LAN IC symbol to WGI217LM QQ4R

X07 01102013
(1) Page 40, change SC106,SC107,SC108,SC109,SC110,SC113,SC114,SC115,SC116 to NI for PARALLEL PORT
(2) Page 42 , change C256,C259,,C262 to 1.5pF,D62 to NI for VGA

X07 01112013
(1) Page 25, add SUSWARN# to SUSACT# Delay Circuit, R1036, R1034, R1038, R1041, R1044, R1048, C639, Q116, Q119, Q120 change to Stuff, R1047 change to 1M, add C682 1uF
(2) Page 17 , change R1560 to NI, for SUSWARN#, SUSACT# delay circuit
(3) Page 24 , change SR51 from 20K ohm to 22.1K ohm for RTCRST# delay

X07 01122013
(1) Page 26 , change SR352 from 249 ohm to 1K ohm for CRB check
Page 4, Change R1621 from 1K to 10K ohm for CRB check

X07 01152013
(1) Page 56 , change SR601 to NI for +1.05V_EN_CTL

X07 01162013
(1) Page 26 , change @U6,@XU6 SPI ROM for support Quad IO

X07 01182013
(1) Page 30&40 , change R1115,BZ301,D61 to NI, change D55 to 1K ohm,R37 to 560 ohm,R38 to 1Kohm for Buzzer Circuit
(2) Page 38 , change MASTA Circuit to NI.
(3) Page 37 , change SU31,SC489,SC491,SR1202,SR1203,SC334,SC490,SC492,C781,C782,C783,C784,C785,C786,C787,C788 to NI for 2 COM change to 1 COM.
(4) Page 40 , change SU38,SC599,SD3,J33,SR679,D54,SC100,SC101,SC102,SC103,SC104,SC105,SC111,SC112 to NI, for LPT Circuit

X07 01212013
(1) Page 04 , change R1273 to 3.24K for VCCST_PWRGD

X07 01222013
(1) Page 53 , change R1309 to 124k ohm for IMON

X07 01282013
(1) Page 38 , change @J15 to NI for MSATA Stanad Off

X08 02012013
(1) Page 38 ,add FB65,FB66 for Msata power option,change SR588,SC545,EC12 to pull MSATA_PWR
(2) Page 40 ,cahge R37, C41 to DGND
(3) Page 30 ,change Audio thermal pad to DGND.change SPK-OUT-L+/- trace width least 15mil
(4) Page 25 ,rename SQ87 to Q10,SR735 to R23,SR737 to R24

X08 02042013
(1) Page P50/P54/P55, Change C25,C48,C49,C52,C53,C102,C110,C111,C846,C865,C873,C874,C919,C920,C921,C945, SC553,SC562,SC668 to standart MLCC for CPU noise

X08 02072013
(1) Page P30, Del reserve Component D1 and D58 for Audio NI Function
(2) Page 38 , change MASTA Circuit to I.
(3) Page 44 , Change SR659 form 300 Ohm to 100 Ohm to adjust LED Light to Meet Lenovo Request

X08 02192013
(1) Page P30, Del reserve Component D2 for Audio NI Function
(2) Page P55, Change SR794,SR797 to 12.4K ohm 1% for +1_5V_DDR OCP

X08 02272013
(1) Page P28, Change R1451,R1452,R1453,R1454,R1455,R1456,R1457,R1459 for HDMI Cost reduced level shifter designs has been updated to 470 ohms (follow 489996_2013WW08_SHB_DT_Denlow_Workstation_MOW_Rev_1_0)
(2) Page P49, change SR863 to 634K ohm,SR834 to 30.9K ohm for Power Meter adjust test function.

A01 03072013
(1) Page 38 , change MASTA Circuit to NI.
(2) Page 53 , R1314 change to 12.1Kohm for L17 thermal protection point.
(3) Page 26/33/46, Change U6,XU6,XU7,SR650,J19,C241 to NI for MP non use.

A01 03202013
(1) Page 17/18/21/26 , change C59,SC47,SC481,SC575,SC634 from Y5V to X7R
(2) Page 30,Base on Lenovo requesr to change AUDIO JACK
(3) Page 14~23/31 , Rpleace Intel PCH and LAN chipset PN [U2&SU10 MFGP/N] for MP

A01 03212013
(1) Page P47, change @Q313 housing Vendor[temperature better than origanl]

A01 03252013
(1) Page P29, Del reserve DP switch SCH for DP Cable NI Function
(2) Page 17, change R1666,R1678,Q436 to NI for ME disable SCH
(3) Page 46, change J9,C241,SR650 to I for Debug Port
(4) Page 24, change E2,R257 to NI for S_RTCRST

A01 03272013
(1) Page 46, change SR650 from 0ohm to 100ohm 1% for Debug Port
(2) Page 43, change SR651 from 120ohm to 47ohm for 3.3V Bleed off circuit have monotonic
(3) Page 25, change SC607 to NI,SR696 200Kohm to 33K ohm for DPWROK sequence fail when AC power Off

A01 03282013
(1) Page 44, change SR659 from 100ohm to 1K ohm,SR660,SR661,SR662 from 300ohm to1K for LED light adjust

A01 03292013
(1) Page 55, change SC664,SC663 from Y5V to X7R
(2) Page 53, change C858,C918,SC646 from Y5V to X7R
(3) Page 37, change C642,SC670 from Y5V to X7R
(4) change C14;C60;C176;C182;C241;C514;C894;C896;C901;C902;C1009;C1027;C1049;C1053;C1067;C1068;SC1;SC148;SC154;SC176;SC178; SC192;SC193;SC194;SC195;SC203;SC205;SC225;SC226;SC231;SC232;SC254;SC255;SC256;SC257;SC281;SC282;SC291;SC328;SC329;SC330; SC331;SC503;SC505;SC515;SC516;SC548;SC549;SC550;SC551;SC574;SC576;SC590;SC602;SC349 from Y5V to X7R

A01 04032013
(1) Page 44, change SR659,SR660,SR661,SR662 from 1k to330 ohm for LED light adjust

A01 04092013
(1) Page 33, change SC716,SC717 18pF to 12pF for SY3 32.768k crystal (SIO)

A01 04112013
(1) Page 4, change U27,R1619,Q336 to NI

A01 04122013
(1) Page 29, change DP solution, U1 vender to TI, SR69 to 0.1uF,SR33,SR65 to NI,R52 to 10K ohm.

A01 04162013
(2) Page 43, change SR651 from 47 ohm to 120 ohm for 3.3V Bleed off circuit have monotonic

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